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AN AREA EFFICIENT CARRY SELECT ADDER

ARCHITECTURE FOR CSLA

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ABSTRACT: Adder plays an important role in any part of the computational systems like addition, subtractions, high speed multiplications, DSPs and ALUs. There are several types of adders like Parallel Adder, Ripple-Carry Adder (RCA), Carry Look-Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSLA) etc. Each adder has their own performance in reducing parameters like area, delay and power. From the structure of CSLA, there is a scope of modifying circuit in turn which increases the speed. Speed is one among the various VLSI parameters which is dealt in this project "Implementation of High Speed Enhanced CSLA Based on Gated D-Latch". From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. The proposed work conveys that it uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular BEC SQRT CSLA architecture. The proposed design has reduced area and power as compared with the regular BEC SQRT CSLA. The proposed design has lesser area owing to the modifications in the BEC unit by gate reduction due to combinational logic. The performance factors of the proposed design are evaluated in terms of delay, area, power and their products by simulation tool and implemented in FPGA kit. The results analysis shows that the proposed modified BEC CSLA structure is better than the regular BEC SQRT CSLA.

Keywords- *Enhanced CSLA (ECSLA), Gated D-Latch, Modified CSLA (MCSLA), Regular CSLA (RCSLA), Xilinx ISE Design Suite 14.4.*

I. INTRODUCTION

In any digital system addition is the fundamental operation. An adder can perform arithmetic operations such as subtraction and logical operations like AND, XOR, XNOR and OR etc. As these adders have the ability to produce those operations it is essential to have a high speed adder. In digital adders, the speed of addition is given by the time taken to forward a carry through the adder. The sum for each bit in an elementary adder is produced sequentially only after the previous bit place was added and a carry is forwarded into the next place.

In the past few years, several adders have been proposed by many members. The carry propagation delay problem which is overcome by independently generating multiple radix carriers, using this carries simultaneously generated sums were selected, which is proposed by O. J. Bedriji. A new scheme is introduced by AkhilashTyagi to generate carry bits with block carry in '1' from the carries of a block with block carry in '0'. T. Y. Chang and M. J. Hsiao proposed add one circuit to replace one RCA instead of using dual RCA in a CSLA scheme. A modified CSLA designed in different stages which reduces the area was proposed by Padma Devi et al. An area efficient VARIABLE CSLA scheme was proposed by Yajuan He et al To reduce the maximum delay the carry is forwarded in to the final stage of Carry Save Adder, Ramkumar et al proposed a Binary to Excess-1 Converter (BEC) method.

The basic idea of this work is to use Gated D-Latch instead of RCA with carry in 1 in RCSLA and BEC in MCSLA. The main benefit of Gated D-Latch is to reduce the delay and achieve high speed CSLA.

In this paper [1], that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using this carries to select between simultaneously generated sums. In this adder system, the addend and augends are divided into sub addend and sub augends sections that are added twice to produce two sub sums. One addition is done with a carry digit forced into each section, and the other addition combines the operands without the forced carry digit. The selection of the correct, or true, sub sum from each of the adder sections depends upon whether or not there actually is a carry into that adder section.

In this paper [2], the design and implementation of a generic fast asynchronous Hybrid Kogge-Stone Structure Carry Select based Adder (HKSS-CSA) is described in detail and its application in the design of asynchronous Double Precision Floating-Point Adder (DPFPA) is presented and the improved latency performance it provides is discussed. A detailed analysis in terms of maximum combinational delay, number of logic levels and logic resources used by both these adders is provided. The proposed HKSS-CSA adder's performance is compared with a generic reference Carry Look-Ahead Adder (CLA) in terms of the parameters.

In this paper [3], that instead of using dual Ripple Carry Adder a Carry Select Adder scheme using an add one circuit to replace one RCA adder requires 29.2% fewer transistors with a speed penalty of 5.9% for bit length 17 = 64. If speed is crucial for this 64bit adder, then two of the original carry-select adder blocks can be substituted by the proposed scheme with area saving and the same speed.

In this paper [4], they introduced a scheme to generate carry bits with block carry in 1 from the carries of a block with block carry in 0. This paper introduces a new reduced-area carry-select scheme where the second copy of the carry-chain is substituted by an 'or' gate per bit position. Replacing the ripple-carry blocks with parallel-prefix blocks results in a select-prefix adder, which has a slightly better area and time than a parallel-prefix adder.

In this paper [5], an adder is introduced to operates with low power and occupies lower area in comparison to conventional CSLA circuit due to using a first zero finder circuit. Besides by three basic changes in the critical path of adder, speed is improved considerably. First of all we used a high speed compact CSLA as partial adder in each block, then a block carry generator (BCG) circuit is used for faster carry propagation and finally we replaced multiplexer gate with a XNOR gate. For designing a fast CSLA, we used combination of conventional CMOS (C-CMOS) and Transmission Gate (TG) logic styles. Also using Complementary Pass-transistor Logic (CPL), due to lower parasitic capacitance, is faster

In this paper [6], an Efficient Novel carry select adder works according to the BEC technique. In this type of Adder, the block of Ripple Carry Adder with input carry as 1 has been replaced with a block of Binary to Excess-1 converter (BEC). The BEC stage is constructed by NMOS stage and also acts as a pass gate. For n-bit ripple carry adder, n+1 bit of Binary to Excess-1 converter is used. This is done in order to reduce the area and power requirement of the previous Carry Select Adder.

II. GATED D-LATCH:

Latches and Flip Flops are the fundamental building blocks of digital electronic systems used in communications, computers and many other systems. Latches are used as data storage elements. A latch is a circuit having two stable states (current state-Q, compliment of current state-Q'). A latch is a Level-Sensitive, where as flip-flops Edge-Sensitive. When a latch is enabled it becomes transparent.

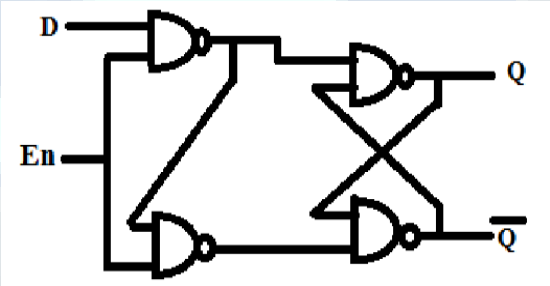

Fig.1: Circuit diagram of Gated D-Latch.

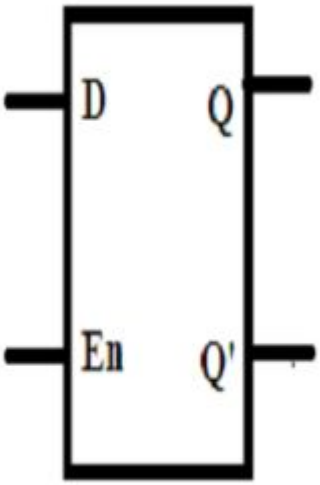

Fig.2: Logic Symbol of Gated D-Latch.

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The Circuit diagram of Gated D-Latch is as shown in fig.1 helps in avoiding the restricted input combinations, which is also known as transparent latch, data latch or gated latch. It has a data input-D and an enable signal-En (we can also use a clock or control signal) as inputs and two stable output states Q and Q'. The word transparent was obtained as the signal propagates directly through the circuit from input-D to the output-Q when the enable input is ON. When enable input is OFF there will be no change. The Logic Symbol of Gated D-Latch is shown in fig.2 and truth table is shown in table1.

Table 1: Truth Table of Gated D-Latch.

En/C	D	Q	Q'	Comments
0	X	QPrevious	Q'Previous	No Change
1	0		1	Reset
1	1		0	Set

III. EXISTING SYSTEM

Carry Select Adder (CSLA)

In RCA every full adder has to wait for the incoming carry before an outgoing carry is generated. One way to get around this linear dependency is to anticipate both possible values of the carry input i.e. 0 and 1 and evaluate the result in advance. Once the real value of the carry is known the result can be easily selected with the help of a simple multiplexer stage.

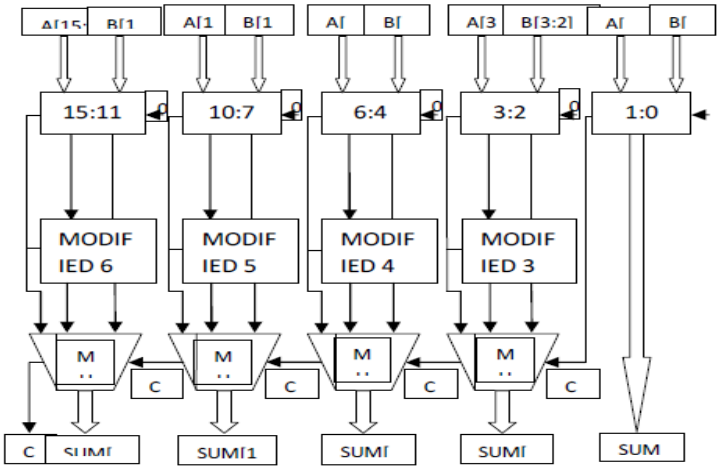

Figure 3: Block Diagram of Carry Select Adder

A 16-bit CSLA is constructed by dividing into 4 stages i.e. N=16 total number of bits, M=4 number of bits per stage, (N/M = 4) and chaining such four equal length blocks as shown in Figure 1.6. CSA has less delay as compared to RCA due to the anticipation of both possible values.

IV. IMPLEMENTATION OF ENHANCED CSLA BASED ON GATED D-LATCH:

The implementation of 64-bit enhanced CSLA based on Gated D-Latch is shown in fig 3. The design was constructed in hierarchical model (top-down design). The 64-bit is divided into two 32-bits and again each 32-bit is divided into two 16 bits.

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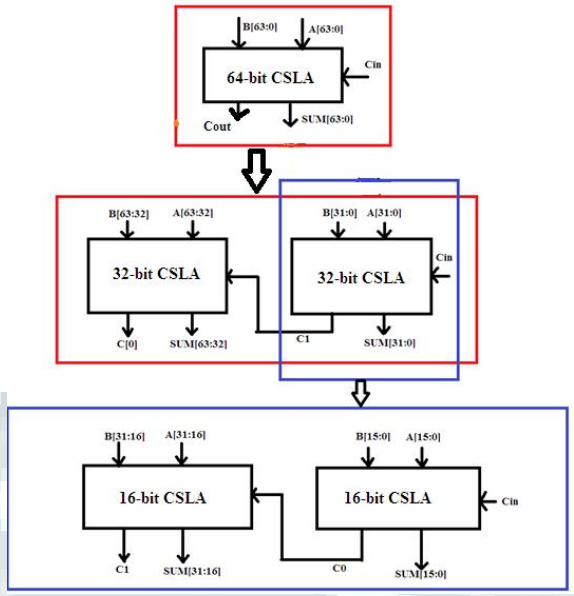

Fig 4: Hierarchy of 64 bit enhanced CSLA based on gated d-latch.

The 16-bit design present in fig 3 is as shown in fig 4; it is again divided into different groups of variable sizes. Each block has some bit length of different sizes. Each block consists of a Ripple Carry Adder (RCA), Gated D-Latch and a multiplexer to each block excluding the block 0, because it is having only one RCA corresponding to that block, so to select the data there is no need of multiplexer.

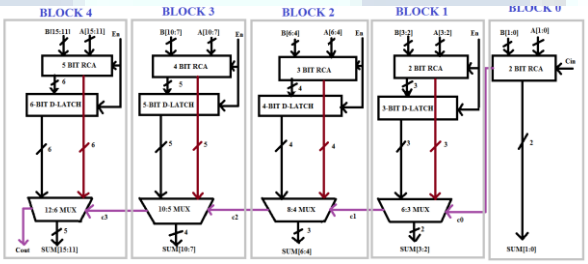

Fig 5:16-bit-Enhanced CSLA based on Gated D-Latch.

The inputs A, B and En are applied. RCA performs two additions as En is a clock signal we get both Logic '0' and Logic '1'. When En is considered as Logic '1' then the RCA performs addition, the obtain Sum from the RCA acts as input to the Gated D-Latch. As discussed before about Gated D-Latch when enable signal is high the output of the Gated D-latch will be same as the input.

When En is considered as Logic '0' then RCA performs addition, the obtain Sum in the RCA will be stored in it only. Now based on the previous block carry the output is selected as either a Gated D-Latch output (when carry= '1') or RCA output (when carry= '0') through the 2:1 mux.

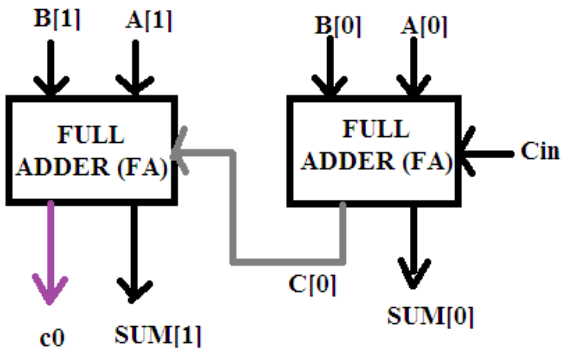

Fig 6: Internal Structure of Block0 of fig 4.

Fig 5 shows the internal structure of block0 of fig 4. It is a 2-bit RCA which contains a series of two full adders in cascade form.

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IV. EXPERIMENTAL RESULTS

4.1 Simulation Results:

The simulation process has been carried out for different levels of abstraction. The simulation has been extended up to our requirement i.e. 64-bit. The code has been written in Verilog hardware description language. The top module has been synthesized and simulated in Xilinx ISE Design Suite 14.4 and the corresponding delay calculations have been noted. By using Gated D-Latch the delay was reduced. Simulation results are shown in fig 12, 13, 14 for 16-bit, 32-bit and 64-bit. RTL Schematic diagrams are shown in fig 15, 16, 17 for 16-bit, 32-bit and 64-bit. The design was implemented in Spartan-3E kit.

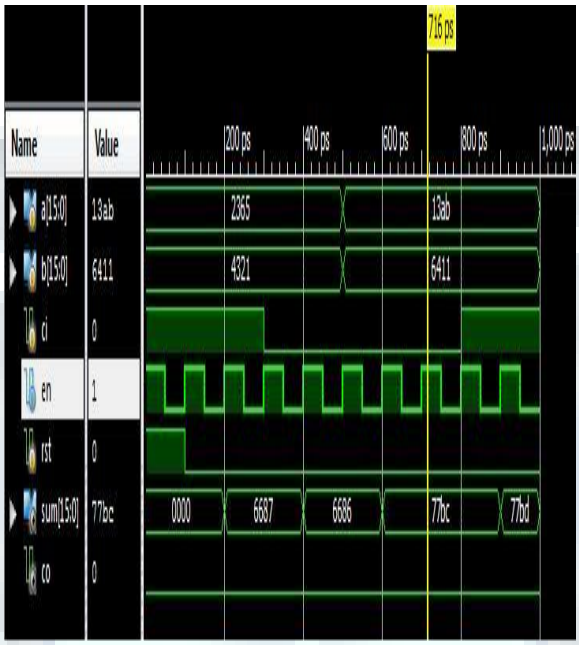

Fig 7: Simulation results of 16-bit Enhanced CSLA using Gated D-Latch.

4.2: RTL (Register Transfer Level) schematic diagrams:

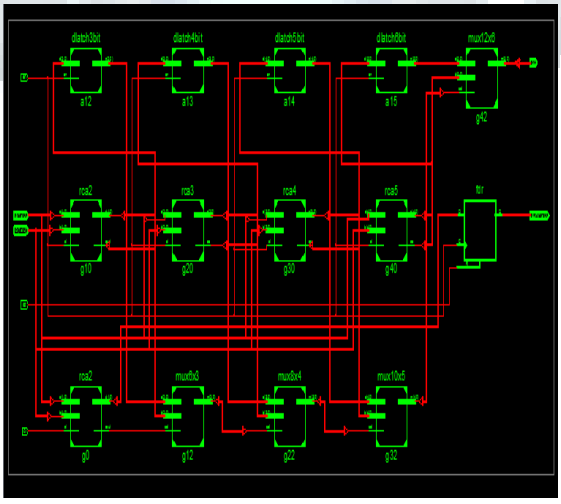

Fig 8: RTL Schematic of 16-bitEnhanced CSLA using Gated D-Latch.

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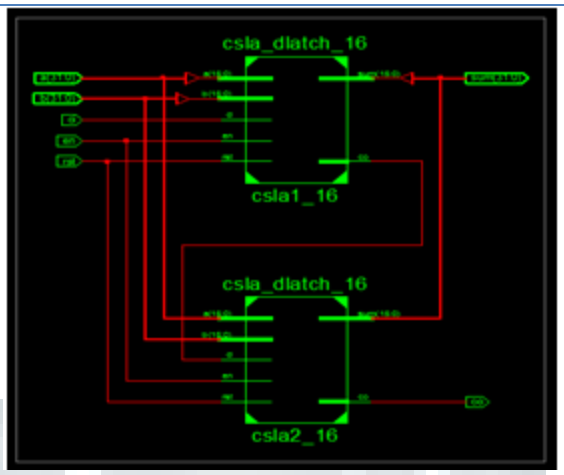

Fig 9: RTL Schematic of 32-bit Enhanced CSLA using Gated D-Latch

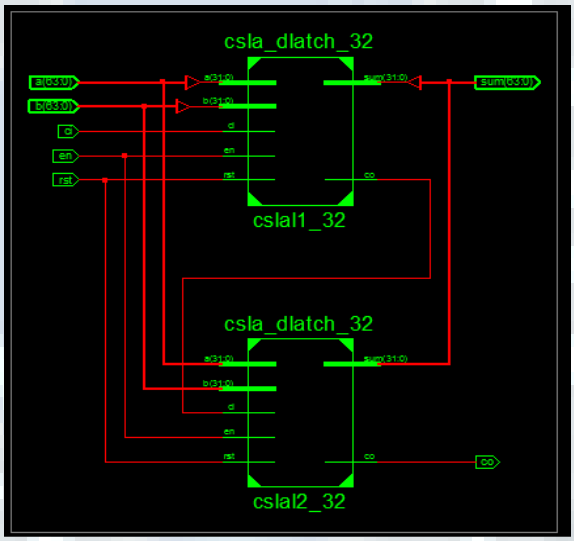

Fig 10: RTL Schematic of 64-bit Enhanced CSLA using Gated D-Latch.

Table V. Comparison Table for Regular, Modified & Enhanced CSLA:

No. Of Bits	DELAY(ns)		
	Regular CSLA	Modified CSLA	Enhanced CSLA
16-Bit	16.204	16.634	14.328
32-Bit	18.257	24.790	18.056
64-Bit	31.535	43.389	20.500

V.CONCLUSION

This paper has really given an effective description on implementation of high speed Gated D-Latch based Enhanced Carry Select Adder (ECSLA). This has been achieved by replacing RCA with carry in "1", by Gated D-Latch which intern helped us to have a new advantageous ECSLA adder than previous adders like RCSLA and MCSLA. Replacing RCA with Gated D-Latch the propagation delay was reduced. The applications of Enhanced Carry Select Adder are used in many electronic applications like calculators, arithmetic logic unit(s) used in processors (like DSP's), computers and are also used where the table indices, addresses are to be calculated faster and where more number of bits are to be added using complex adders for signed number representations. The Proposed work provides an efficient adder for arithmetic operations by using

the Modified Carry Select Adder. Comparing it to the conventional design it has an advantage of area reduction by less number of gates and low power circuit. Considerably the delay is also reduced by modified CSLA. The gate counts are reduced by modifying the Binary to Excess One Converter unit and the Ripple Carry Adder unit by simplifying using AOI logic. The proposed CSLA is implemented for different Word sizes. The proposed design may be suitable for low power applications such as Filter design, Multipliers and digital signal processing. Future scope of this project is, new types of adders can be developed in place of RCA and there by the area and delay of the adders can be decreased as the number of bits increases simultaneously.

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