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IMPLEMENTATION OF ENERGY EFFICIENT VEDIC MATHEMATICS MULTIPLIER

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***Abstract*:** A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents a high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift. The most significant aspect of the proposed method is that, the developed multiplier architecture is based on Vertical and Crosswise structure of Ancient Indian. Vedic Mathematics Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. Vedic Mathematics has a unique technique of calculations based on 16 Sutras. This paper presents study on high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift. Further, the Verilog HDL coding of Urdhva tiryakbhyam Sutra for 8x8 bits multiplication and their FPGA implementation by Xilinx Synthesis Tool on Spartan 3 kit have been done and output has been displayed on LED's of Spartan 3 kit.

***Index Terms* :-** *Architecture, Ripple Carry (RC) Adder, Multiplication, Vedic Mathematics, Vedic Multiplier (VM), Urdhava Tiryakbhyam Sutra.*

I. INTRODUCTION

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. We discuss a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Triyakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. In this paper, after a gentle introduction of this Sutra, it is applied to the binary number system to make it useful in the digital hardware. The hardware architecture of the Vedic multiplier is presented and is shown to be very similar to that of the popular array multiplier. It is also equally likely that many such similar technical applications might come up from the storehouse of knowledge, Veda, if investigated properly [1-3].

Pipeline architecture based on the constant geometry radix-2 FFT algorithm, which uses log2N complex-number multipliers (more precisely butterfly units) and is capable of computing a full N-point FFT in N/2 clock cycles, has been proposed by J.Choi and V.Boriakoff. However, this architecture requires a large amount of delay elements (memory size of N.log2N samples) and a quite complicated switching mechanism for the routing of the data [4].

In the present age of digital communication various audio visual or any other perception signals are sampled on time [i.e. axis] and are quantized on amplitude [y- axis], to produce discrete version of the continuous signal .This results in the corresponding information being contained in a series of binary (0 & 1) sequence. Hence any processing or transformation of original signal boils down to suitable discrete mathematical operation applied to binary sequences [5-6]. Different algorithms exist to accomplish each of these tasks. The task themselves may include basic arithmetic operations like addition, subtraction, multiplication, division, matrix, squaring, exponential operations etc. While implementing these algorithms on digital computer, the prevalent VAN-NEUMAN architecture uses registers operations like shift, move, Compliment, add etc. to accomplish these basic arithmetic tasks. The actual CPU implementation of these operations is through suitable amalgamation of algorithm and implementing architecture. Though there are many algorithms for the same task only VAN-NEUMAN architectural implementation of classical method is found to be used in present day digital computers. The Vedic mathematical methods suggested by

Shankaracharya Sri. Bharti Krishna Tirtha through his book offer efficient alternatives.

The intermediate stages include several comparisons, additions and subtractions which reduce the speed exponentially with the total number of bits present in the multiplier and the multiplicand. Since speed is our major concern, utilizing such type of architectures is not a feasible approach since it involves several time consuming operations.

In order to address the disadvantages with respect to speed of the above mentioned methods, and explored a new approach to multiplier design based on ancient Vedic Mathematics. Vedic Mathematics is an ancient and eminent approach which acts as a foundation to solve several mathematical challenges encountered in the current day scenario. Vedic Mathematics existed in ancient India and was rediscovered by a popular mathematician, Sri Bharati Krishna Tirthaji. He bifurcated Vedic mathematics into 16 simple sutras (formulae). These Sutras deal with Arithmetic, Algebra, Geometry, Trigonometry, Analytical Geometry etc. The simplicity in the Vedic mathematics sutras paves way for its application in several prominent domains of engineering like Signal Processing, Control Engineering and VLSI .

One of the highlights of the Vedic maths approach is that the calculation of all the partial products required for multiplication, are obtained well in advance, much before the actual operations of multiplication begin. These partial products are then added based on the Vedic maths algorithm to obtain the final product. This in turn leads to a very high speed approach to perform multiplication.

In this, we explore a method to further enhance the speed of a Vedic mathematics multiplier by replacing the existing full adders and half adders of the Vedic mathematics based multipliers with compressors. Compressors, in its several variants, are logic circuits which are capable of adding more than 3 bits at a time as opposed to a full adder and capable of performing this with a lesser gate count and higher speed in comparison with an equivalent full adder circuit.

II. VEDIC - MATHS

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda.

It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamhiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. The very word „Veda" has the derivational meaning i.e. the fountainhead and illimitable storehouse of all knowledge. Vedic mathematics is the name given to the ancient system of mathematics or, to be precise a unique technique of calculations based on simple rules and principles with which many mathematical problems can be solved, be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

Let us consider two 8 bit numbers X7 -X0 and Y7-Y0, where 0 to 7 represent bits from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). P0 to P15 represent each bit of the final computed product. It can be seen from equation (1) to (15), that P 0 to P15 are calculated by adding partial products, which are calculated previously using the logical AND operation. The individual bits obtained from equations (1) to (15), in turn when concatenated produce the final product of multiplication which is depicted in (16).The carry bits generated during the calculation of the individual bits of the final product are represented from C1 to C30. The carry bits generated in (14) and (15) are ignored since they are superfluous.

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$P_0 = A_0 * B_0$	(1)
$C_1P_1 = (A_1 * B_0) + (A_0 * B_1)$	(2)
$C_3C_2P_2 = (A_2 * B_0) + (A_0 * B_2) + (A_1 * B_1) + C_1$	(3)
$C_5C_4P_3 = (A_3 * B_0) + (A_2 * B_1) + (A_1 * B_2) + (A_0 * B_3)$	(4)
$C_7C_6P_4 = (A_4 * B_0) + (A_3 * B_1) + (A_2 * B_2) + (A_1 * B_3) + (A_0 * B_4) + C_3 + C_4$	(5)
$C_{10}C_9C_8P_5 = (A_5 * B_0) + (A_4 * B_1) + (A_3 * B_2)$	(6)
$C_{13}C_{12}C_{11}P_6 = (A_6 * B_0) + (A_5 * B_1) . (A_4 * B_2)$	(7)
$+ (A_3 * B_3) + (A_2 * B_4) + (A_1 * B_5) + (A_0 * B_6) + C_7 + C_8$	
$C_{16}C_{15}C_{14}P_7 = (A_7 * B_0) + (A_6 * B_1) + (A_5 * B_2) + (A_4 * B_3) + (A_2 * B_5) + (A_1 *$	(8)
$C_{19}C_{18}C_{17}P_8 = (A_7 * B_1) + (A_6 * B_2) + (A_5 * B_3) + (A_4 * B_4) + (A_3 * B_5) + (A_2 * B_6) + (A_1$	(9)
$C_{22}C_{21}C_{20}P_9 = (A_7 * B_2) + (A_6 * B_3) + (A_5 * B_4) + (A_4 * B_5) + (A_3 * B_6) + (A_2 * B_7) + C_{13}$	(10)
$C_{25}C_{24}C_{23}P_{10} = (A_7 * B_3) + (A_6 * B_4) + (A_5 * B_5) + (A_4 * B_6) + (A_3 * B_7) + C_{16} + C_{18} + C_{20}$	(11)
$C_{27}C_{26}P_{11} = (A_7 * B_4) + (A_6 * B_5) + (A_5 * B_6)$	(12)
$C_{29}C_{28}P_{12} = (A_7 * B_5) + (A_6 * B_6) + (A_5 * B_7)$	(13)
$C_{30}P_{13} = (A_7 * B_6) + (A_6 * B_7) + C_{25} + C_{27} + C_{28}$	(14)
$P_{14} = (A_7 * B_7) + C_{29} + C_{30}$	(15)
$P_{15} = (A_7 * B_7)$	(16)

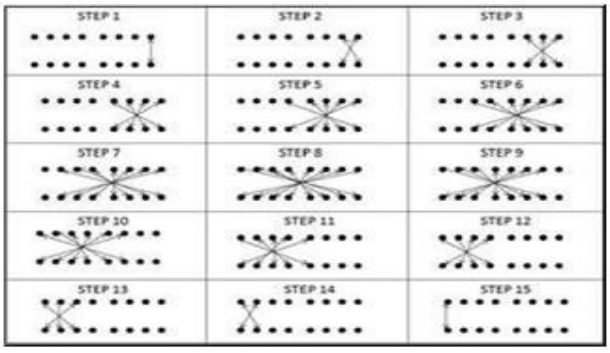

Fig 1. Pictorial Illustration of Urdhwa Tiryakbhyam Sutra for multiplication of 2 eight bit numbers

Fig.1 illustrates the step by step method of multiplying two 8 bit numbers using the Urdhwa Tiryakbyam Sutra. The black circles indicate the bits of the multiplier and multiplicand, and the two-way arrows indicate the bits to be multiplied in order to arrive at the individual bits of the final product. The hardware architecture of the 8x8 Urdhwa multiplier has been designed and shown in Fig. 2.

As mentioned earlier, the partial products obtained are added with the help of full adders and half adders. It can be seen, from equation (1) to (16) that in few equations there is a necessity of adding more than 3 bits at a time. This leads to additional hardware and additional stages, since the full adder is capable of adding only 3 bits at a time. In the next section two different types of compressor architectures are explored which assist in adding more that 3 bits at a time, with reduced architecture and increased efficiency in terms of speed.

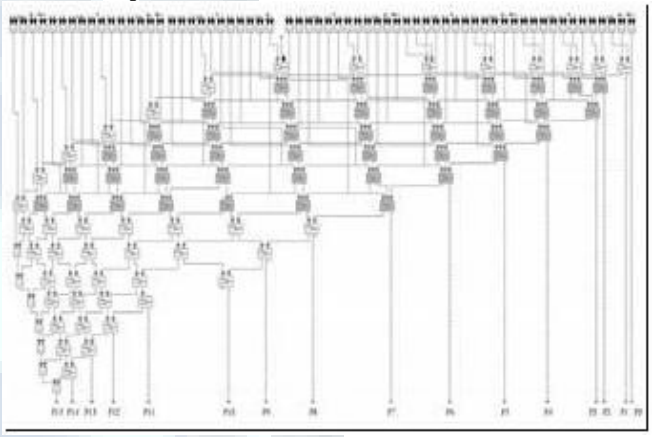

Fig. 2. Hardware architecture of Urdhva Tiryakbhyam multiplier where the colored blocks represent the full adders and the white colored blocks represent the half adders.

III. IMPLEMENTATION OF MULTIPLIER USING VM ALGORITHM

Multiplication methods are extensively discussed in Vedic mathematics. Various tricks and short cuts are suggested by VM to optimize the process. These methods are based on concept of 1 Multiplication using deficits and excess 2 Changing the base to simplify the operation. Various methods of multiplication proposed in VM

a) UrdhvaTiryagBhyam - vertically and crosswise

b) Nikhilam navatashcharamam Dashatah: All from nine and last from ten

c) Anurupyena: Proportionately Vinculum

IV. URDHVA TIRYAGBHYAM

Urdhva – Triyakbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It means vertically and crosswise. We discuss multiplication of two, 4 digit numbers with this method [8-9]. Ex.1. the product of 1111

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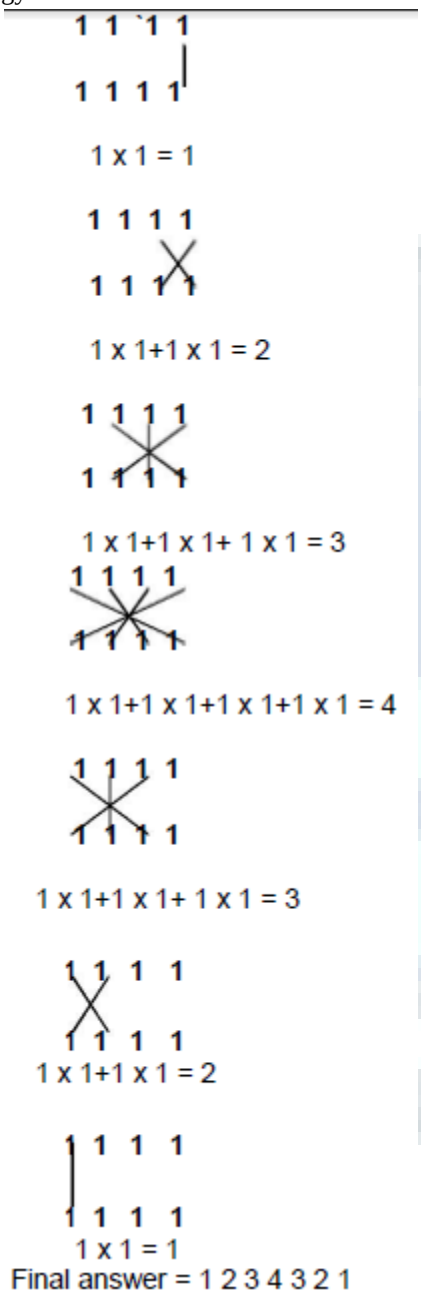
and 1111 using *Triyakbhyam* (vertically and crosswise) is given below.

Methodology of Parallel Calculation



V. MULTIPLIER ARCHITECTURE

The hardware architecture of 2X2, 4x4 and 8x8 bit Vedic multiplier module are displayed in the below sections. Here, "Urdhva-Tiryagbhyam" (*Vertically and Crosswise*) sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work.

A. Vedic Multiplier for 2x2 bit Module

The method is explained below for two, 2 bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0 as shown in Fig. 2. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit Of the finel product. The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Fig. 3. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier [2]. Hence it is concluded that multiplication of 2 bit binary numbers by Vedic method does not made significant effect in improvement of the multiplier"s efficiency. Very precisely we can state that the total delay is only 2-half adder delays, after final bit products are generated, which is very similar to Array multiplier. So we switch over to the implementation of 4x4 bit Vedic multiplier which uses the 2x2 bit multiplier as a basic building block. The same method can be extended for input bits 4 & 8. But for higher no. of bits in input, little modification is required.

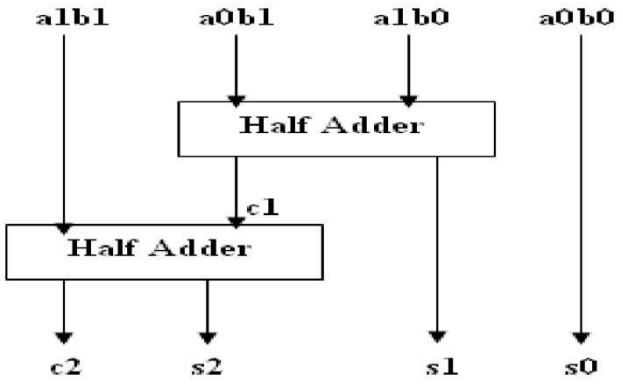
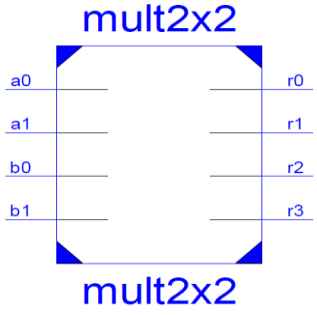


Fig. 3 Block Diagram of 2x2 bit Vedic Multiplier



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Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2	5888	0%
Number of 4 input LUTs	4	11776	0%
Number of bonded IOBs	8	372	2%

B. Vedic Multiplier for 4x4 bit Module

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig. 3. Let"s analyze 4x4 multiplications, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for the multiplication result is – S7S6S5S4 S3 S2 S1 S0 .Let"s divide A and B into two parts, say A3A2 & A1 A0 for A and B3 B2 & B1B0 for B. Using the fundamental of Vedic multiplication, taking two bit at a timeand using 2 bit multiplier block, we can have the following structure for multiplication as shown in Fig. 4.

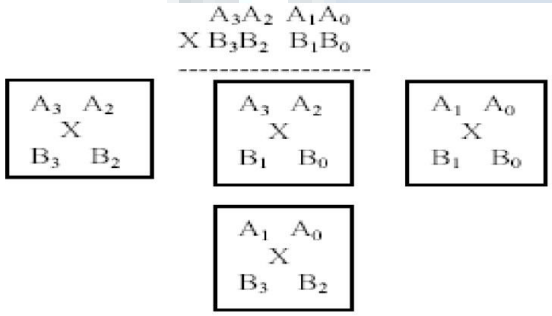

Fig. 4 Sample Presentation for 4x4 bit Vedic Multiplication Each block as shown above is 2x2 bit Vedic multiplier. First 2x2 bit multiplier inputs are A1A0 and B1B0. The last block is 2x2 bit multiplier with inputs A3 A2 and B3 B2. The middle one shows two 2x2 bit multiplier with inputs A3 A2 & B1B0 and A1A0 & B3 B2. So the final result of multiplication, which is of 8 bit, S7 S6S5S4 S3 S2 S1 S0. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Fig. 5. To get final product (S7 S6 S5 S4 S3 S2 S1 S0), four 2x2 bit Vedic multiplier (Fig. 3) and three 4-bit Ripple-Carry (RC) Adders are required. The proposed Vedic multiplier can be used to reduce delay. Early literature speaks about Vedic multipliers based on array multiplier structures. On the other hand, we proposed a new architecture, which is efficient in terms of speed. The arrangements of RC Adders shown in Fig. 5, helps us to reduce delay. Interestingly, 8x8 Vedic multiplier modules are implemented easily by using four 4x4 multiplier modules.

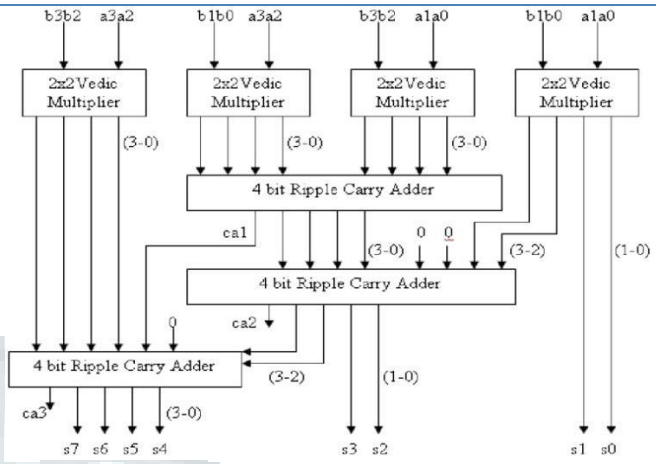

Fig. 5 Block Diagram of 4x4 bit Vedic Multiplier

C. Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 6 can be easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section Let"s analyze 8x8 multiplications, say A= A7 A6 A5 A4 A3 A2 A1 A0 and B= B7 B6 B5B4 B3 B2 B1B0. The output line for the multiplication result will be of 16 bits as – S15 S14 S13 S12 S11 S10 S9 S8 S7 S6bS5S4 S3 S2 S1 S0. Let"s divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as: Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total three 8 bit Ripple-Carry Adders are required as shown in Fig. 6.

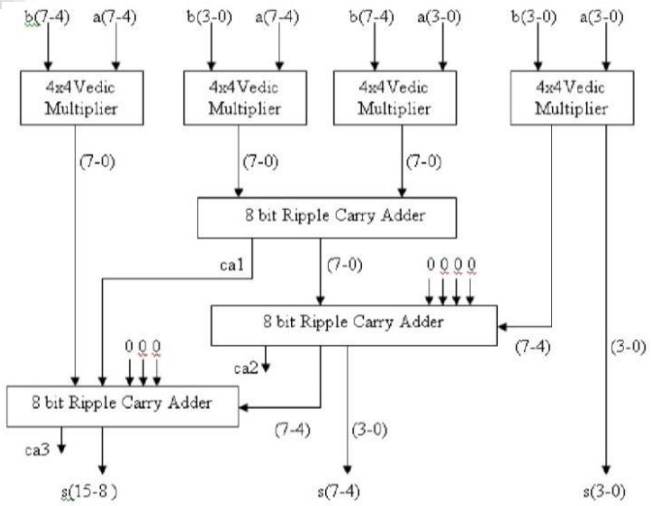

Fig. 6 Block Diagram of 8x8 bit Vedic Multiplier

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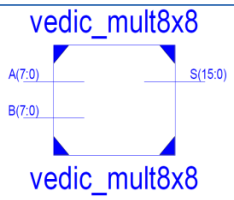

Implementation Design for 8x8

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	101	5888	1%
Number of 4 input LUTs	176	11776	1%
Number of bonded IOBs	32	372	8%

Simulation output of the 8x8 Multiplier For the value 8h and 7h gives a result in hexadecimal 38 .

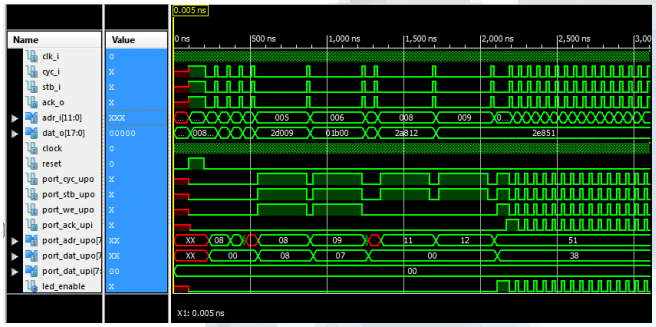

Table 1 Comparison of 8x8 bit Multipliers (in ns)

D. Generalized Algorithm for N x N bit Vedic Multiplier

We can generalize the method as discussed in the previous sections for any number of bits in input. Let, the multiplication of two N-bit binary numbers (where N = 1, 2, 3…N, must be in the form of 2N) *A* and *B* where A = AN.....A3 A2 A1 and B = BN….B3 B2 B1. The final multiplication result will be of (N + N) bits as S = S(N + N)....S3 S2 S1.

Step 1: Divide the multiplicand A and multiplier B into two equal parts, each consisting of [N to (N/2)+1] bits and [N/2 to 1] bits respectively, where first part indicates the MSB and other represents LSB.

Step 2: Represent the parts of A as AM and AL, and parts of B as BM and BL. Now represent A and B as AM AL and BM BL respectively.

Step 3: For A X B, we have general format as shown in Fig.7

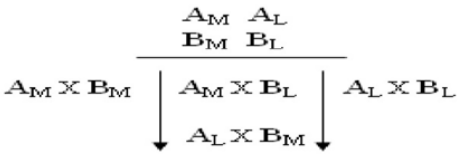

Fig. 7 General Representation for vedic multiplication

VI. CONCLUSION & FUTURE WORK

This paper presents a highly efficient method of multiplication – "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. It gives us method for hierarchicalmultiplier design and clearly indicates the computational advantages offered by Vedic methods. The computational path delay for proposed 8x8 bit Vedic multiplier is found to be 21.679 ns. Hence our motivation to reduce delay is finely fulfilled. In this paper, we have proposed a novel high speed architecture for multiplication of two 8 bit numbers, combining the advantages of compressor based adders and also the ancient Vedic maths methodology. New 7:2 compressor architecture, based on 4:2 compressor architecture was also discussed.It is observed that the Vedic multiplier is much more efficient than Array and Booth multiplier in terms of execution time (speed). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education.

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