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VLSI IMPLEMENTATION OF AREA, DELAYANDPOWER EFFICIENT MULTISTAGE SQRT-CSLA ARCHITECTURE DESIGN

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ABSTRACT: The arithmetic operations involved in carry select adder (CSLA) and binary to Excess-1 converter (BEC) - based CSLA are analysed.CSLA has great scope by reducing area, delay and power consumption. However the regular CSLA is still area consuming due to dual ripple carry adder (RCA) structure, for reducing the area.CSLA can be implemented by using single RCA and BEC converter. In proposed architecture I present and innovated multistage SQRT-CSLA architecture. The substantiation of the proposed design is done through design and implementation of 16-bit adder circuit with multipath carry propagation feature. Simulated results show that the proposed architecture achieves two advantages that is 48% less ADP and 50% less power consumption. Than the CSLA and CSLA with BEC.For simulation Xilinx ISE is used. . In this paper, conventional CSLA is compared with Modified Carry select adder (MCSLA), Regular Square Root CSLA (SQRT CSLA), Modified SQRT CSLA and Proposed SQRT CSLA in terms of area, delay and power consumption. The result analysis shows that the proposed structure is better than the conventional CSLA.

Keywords*: Adder, Carry select Adder (CSLA), Modified CSLA (MCSLA), Square Root CSLA (SQRT CSLA), Data processing processors.*

I.INTRODUCTION

In many computers and other kind of processors, adders are not only used in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar applications. Some other applications of adders are in Multiply – Accumulate (MAC) structures. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR. Now a days, design of low power, area efficient high speed data path logic systems are the most substantial areas in the research of VLSI design.

On the basis of requirements such as area, delay and power consumption some of the complex adders are Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer. Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder.[1]

This paper presents a comparative analysis of various adders and proposed design of SQRT CSLA by sharing Common Boolean Logic and modified CSLA using Binary to Excess-1 Converter (BEC). Both these adders show less area, delay and power than other adders.

The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [5], [6]. The delay and area evaluation methodology of the regular and modified SQRT CSLA are presented respectively.

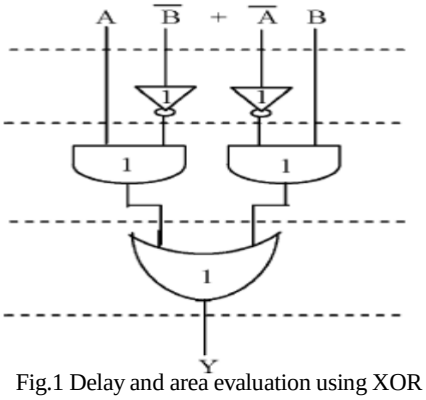

Fig.1 Delay and area evaluation using XOR gate

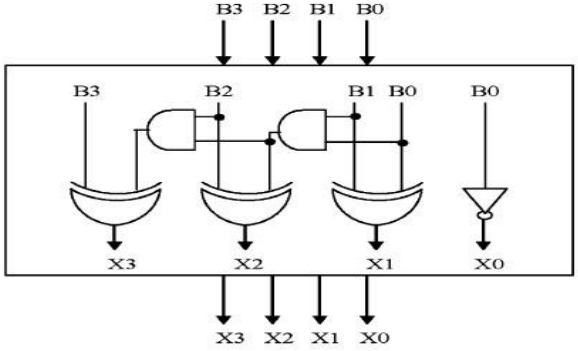

Fig. 2.4-b BEC.

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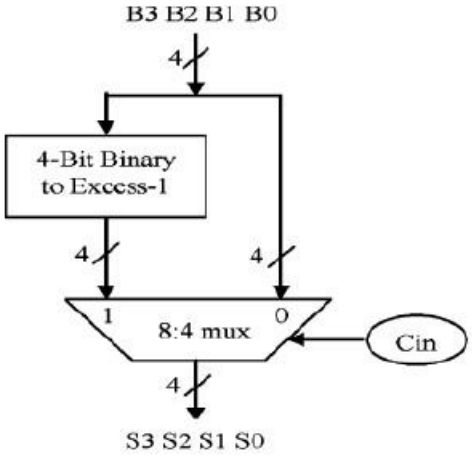

Fig. 3. 4-b BEC with 8:4 mux

II. LITERATURE SURVEY

Ripple Carry Adder consists of cascaded "N" single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Fig. 1 shows the block diagram of ripple carry adder. Now as the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. Now CSLA provides a way to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage. Therefore the conventional CSLA makes use of Dual RCA's to generate the partial sum and carry by considering input carry Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers. Fig. 2 shows the 16-bit Conventional CSLA.

The conventional CSLA is area consuming due to the use of dual RCA's.

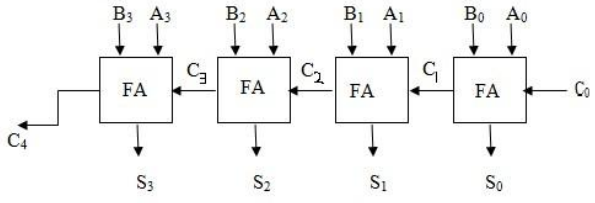

Fig. 4 4-bit Ripple Carry Adder

The basic idea of this work is to use Binary to Excess- 1 converter (BEC) instead of RCA with Cin=1 in conventional CSLA in order to reduce the area and power. [2][3] BEC uses less number of logic gates than N-bit full adder structure. To replace N-bit RCA, an N+1 bit BEC is required. Therefore, Modified CSLA has low power and less area than conventional CSLA. SQRT CSLA has been chosen for comparison with modified design using BEC as it has more balanced delay, less area and low power [4]. Regular SQRT CSLA also uses dual RCAs. In order to reduce the delay, area and power, the design is modified by using BEC instead of RCA with Cin=1. Therefore, the modified SQRT CSLA occupies less area, delay and low power. Further also, the parameters like delay, area and power can be reduced.

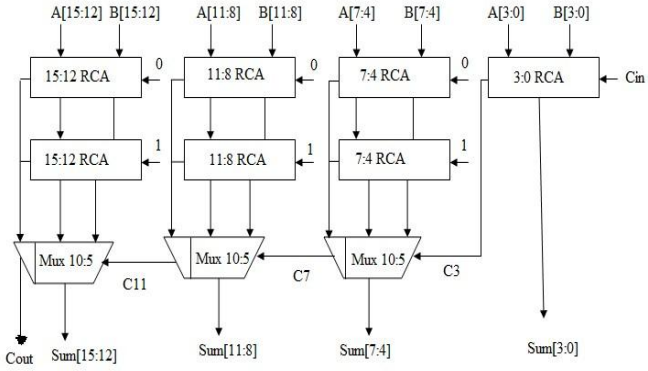

Fig. 5. 16-bit conventional carry select adder

By sharing Common Boolean Logic (CBL), a circuit of SQRT CSLA is proposed. This proposed design is better than all the other adders in respect of area, delay and power consumption.

III. MODIFIED CSLA

The main idea of this work is to use BEC instead of RCA with carry C_{in}=1 in order to reduce the area and power of conventional CSLA. BEC [3] is a circuit used to add 1 to the input numbers. Circuit of BEC is shown in Fig. 3. And truth table is shown in Table I. Goal of addition is achieved using BEC together with the multiplexer as shown in Fig. 4.One of the input of 8:4 MUX gets as its inputs(B3,B2,B1 and B0) and another input of MUX is BEC output. Boolean expressions of 4-bit BEC are listed below (Note: symbols

~NOT, &AND and ^XOR) X0= ~B0

X1= B0^B1

X2= B2^(B0&B1)

X3= B3^(B0&B1&B2)

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TABLE I

TRUTH TABLE OF 4-BIT BINARY TO EXCESS-1 CONVERTER

Binary Logic $B_0 B_1 B_2 B_3$	Excess-1 Logic $X_0 X_1 X_2 X_3$
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

The main idea of this work is to use BEC instead of RCA with Cin=1 in order to get the reduced area and power consumption of the conventional CSLA. To replace the N-bit RCA, N+1 bit BEC is required.

Thus, modified CSLA is designed such that it occupies less area and has low power than conventional CSLA. Block diagram of Modified CSLA is shown in Fig. 5.

IV. REGULAR SQRT CSLA AND MODIFIED SQRT CSLA

The structure of 16-bit regular SQRT CSLA is shown in Fig.6. It has five groups of different size RCA. Each group contains dual RCA and MUX. Conventional CSLA has one main disadvantage of high area usage. This advantage can be overcome in Regular SQRT CSLA. So SQRT CSLA is improved version of Conventional CSLA. Time delay of conventional CSLA can be decreased by having one more input into each set of adders than in previous set. This is known as SQRT CSLA. In SQRT CSLA, group3 has two sets of 3-bit RCA. Selection input of 8:4 MUX is c3.If c3=0, then MUX selects first RCA output(Cin=0) otherwise second RCA output(Cin=1) is selected.

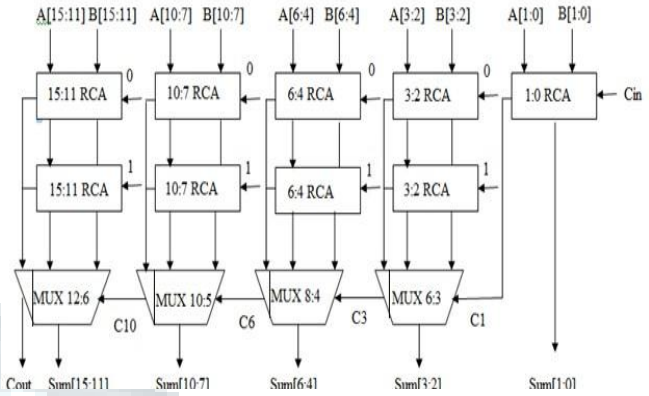

Fig.6 Regular 16-bit SQRT CSLA

Modified SQRT CSLA is similar to that of regular SQRT CSLA, the only difference is we replace RCA with Cin=1 with BEC. This replaced BEC performs the same operation as that of the replaced RCA with Cin=1. Fig. 7 shows the block diagram of modified SQRT CSLA. This structure consumes less area, delay and power than regular SQRT CSLA because of less number of transistors are used.

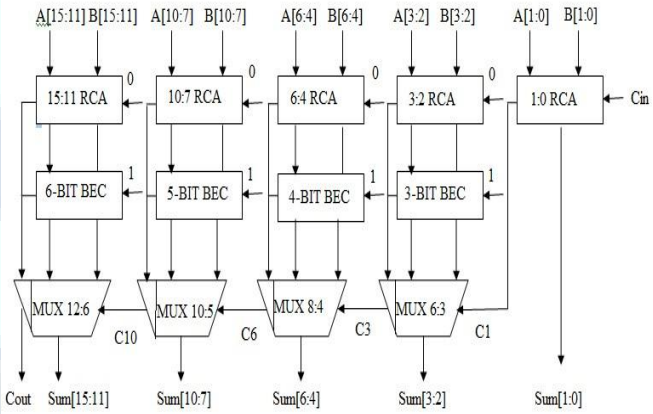

Fig. 7 Modified 16-bit SQRT CSLA

V. PROPOSED SQRT CSLA USING COMMON BOOLEAN LOGIC

To remove the duplicate adder cells in the conventional CSLA, an area efficient SQRT CSLA is proposed by sharing Common Boolean Logic (CBL) term. While analysing the truth table of single bit full adder, results show that the output of summation signal as carry-in signal is logic "0" is inverse signal of itself as carry-in signal is logic "1". It is illustrated by red circles in Table II. To share the Common Boolean Logic term, we only need to implement a XOR gate and one INV gate to generate the summation pair. And to generate the carry pair, we need to implement one OR gate and one AND gate. In this way, the summation and carry circuits can be kept parallel.

TABLE III

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TRUTH TABLE OF SINGLE BIT FULL ADDER, WHERE THE UPPER HALF PART IS THE CASE OF CIN=0 AND THE LOWER HALF PART IS THE CASE OF CIN=1

Cin	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

This method replaces the Binary to Excess-1 converter add one circuit by common Boolean logic. As compared with modified SQRT CSLA, the proposed structure is little bit faster. Internal structure of proposed CSLA is shown in Fig. 8.

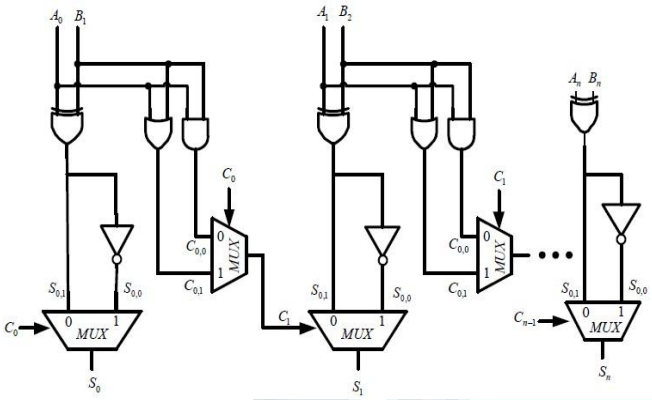

Fig. 8 Internal structure of the proposed area-efficient carry select adder is constructed by sharing the common Boolean logic term

In the proposed SQRT CSLA, the transistor count is trade-off with the speed in order to achieve lower power delay product. Thus the proposed SQRT CSLA using CBL is better than all the other designed adders. Fig. 9 shows the block diagram of Proposed SQRT CSLA.

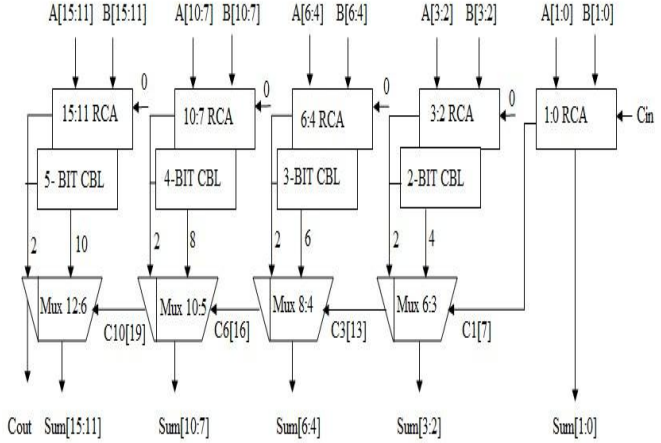

Fig. 9 16-Bit Proposed SQRT CSLA using Common Boolean Logic

VI. RESULTS

This work has been developed using Xilinx tool. Table III shows the comparison between the various adders like conventional CSLA, Modified CSLA, regular SQRT CSLA, modified SQRT CSLA and proposed SQRT CSLA for 8-bit, 16-bit, 32-bit and 64-bit. The parameters on which they are compared are area, delay and power. Fig. 10 depicts that the proposed SQRT CSLA has less number of gates and hence less area. Fig. 11 shows the adder circuit for delay comparison. The results compared in Fig. 12 shows that the power consumption of proposed SQRT CSLA is reduced. It is clear that power, area and delay of proposed SQRT CSLA for 8-bit, 16-bit, 32-bit and 64-bit is reduced as compared to other adders.

TABLE II

COMPARISON OF ADDERS FOR AREA, DELAY, POWER AND POWER DELAY PRODUCT

Word Size	Adder	Area (No. of gate count)	Delay (ns)	Power (mW)	Power Delay Product (pWs)
8-bit	Conventional (Dual RCA)	200	14.46	94.48	1366.36
	Modified (with BEC)	167	16.63	86.92	1445.47
	Regular SQRT (Dual RCA)	144	11.92	193	2300.56
	Modified SQRT(with BEC)	132	13.69	180	2464.2
	Proposed SQRT(with CBL)	111	11.15	119	1326.85
16-bit	Conventional (Dual RCA)	480	19.81	94.63	1874.90
	Modified (with BEC)	381	21.59	81.38	1757.48
	Regular SQRT (Dual RCA)	348	16.15	315	5087.25
	Modified SQRT(with BEC)	291	18.77	268	5030.36
	Proposed SQRT(with CBL)	276	15.48	177	2739.96
32-bit	Conventional (Dual RCA)	1040	30.51	95.01	2899.42
	Modified (with BEC)	809	32.65	79.81	2605.79
	Regular SQRT (Dual RCA)	698	28.97	553	16020.41
	Modified SQRT(with BEC)	762	34.44	448	15429.12
	Proposed SQRT(with CBL)	552	26.23	321	8419.23
64-bit	Conventional (Dual RCA)	2160	51.92	95.49	4958.222
	Modified (with BEC)	1665	54.01	79.25	4280.292
	Regular SQRT (Dual RCA)	1592	52.82	860	45425.2
	Modified SQRT(with BEC)	1498	64.61	745	48134.45
	Proposed SQRT(with CBL)	1104	47.74	555	26495.7

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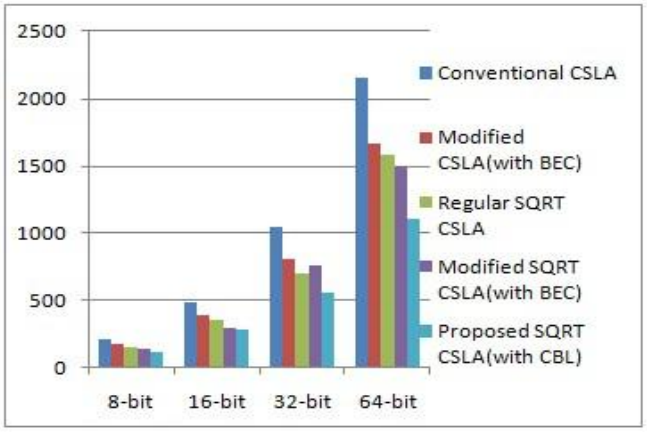

Fig. 10 Comparison of adders for area (no. of gate count)

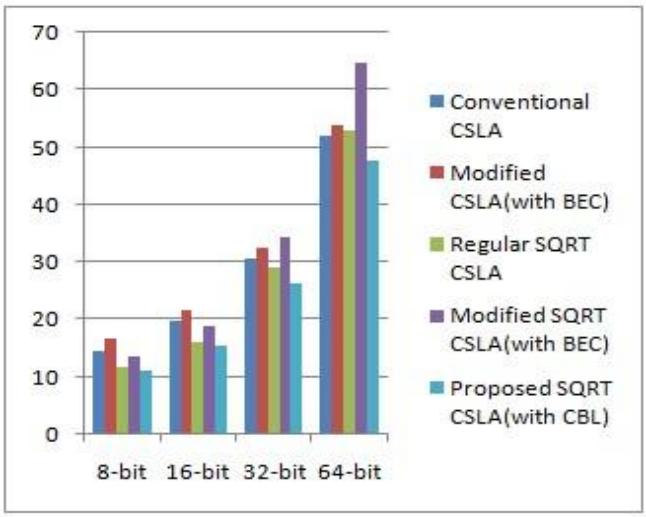

Fig. 11 Comparison of adders for delay

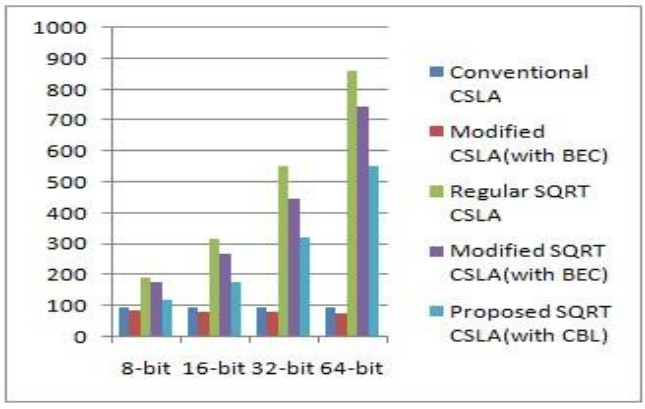

Fig. 12 Comparison of adders for power

VII. CONCLUSION

Power, delay and area are the constituent factors in VLSI design that limits the performance of any circuit. This work presents a simple approach to reduce the area, delay and power of CSLA architecture. The conventional carry select adder has the disadvantage of more power consumption and occupying more chip area. The proposed SQRT CSLA using common Boolean logic has low power, less delay and reduced area than all the other adder structures. It is also little bit faster than all the other adders. In this way, the transistor count of proposed SQRT CSLA is reduced having less area and low power which makes it simple and efficient for VLSI hardware implementations.

VIII. FUTURE SCOPE

This work has been designed for 8-bit, 16-bit, 32-bit and 64- bit word size and results are evaluated for parameters like area, delay and power. This work can be further extended for higher number of bits. New architectures can be designed in order to reduce the power, area and delay of the circuits. Steps may be taken to optimize the other parameters like frequency, number of gate clocks, length etc.

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