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NOVEL HIGH SPEED VEDIC MATHEMATICS MULTIPLIER USING REVERSIBLE LOGIC

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Abstract: Among the various methods of multiplication in Vedic mathematics, Urdhva tiryagbhyam, being a general multiplication formula, is equally applicable to all cases of multiplication. This is more efficient in the multiplication of large numbers with respect to speed and area. In this paper, a 4 X 4 binary multiplier is de-signed using this sutra. A new 4-bit adder is proposed which when used in multiplier, reduces its delay. This multiplier can be used in applications such as digital signal processing, encryption and decryption algorithms in cryptography, and in other logical computations. This design is simulated using VHDL. Currently the speed of the multipliers is limited by the speed of the adders used for partial product addition. In this paper, we proposed an 8-bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) for generating the partial products. The partial product addition in Vedic multiplier is realized using carry-skip technique. An 8-bit multiplier is realized using a 4-bit multiplier and modified ripple carry adders. In the proposed design we have reduced the number of logic levels, thus reducing the logic delay. Simulation of the architecture is carried out using Xilinx ISIM and synthesized using Xilinx XST. Results indicate 13.65% increase in the speed when compared to normal Vedic multiplier.

Index Terms : Vedic Multiplier, cryptography, Digital signal processing, *Reversible Logic, Nikhilam Sutra, vedic multiplier, Quantum cost, Total reversible logic implementation cost*.

I.INTRODUCTION

Vedic mathematics is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krishna Tirtha after his research on Vedas . He constructed 16 sutras and16 upa sutras after extensive research in Atharva Veda. The most famous among these 16 are Nikhilam Sutram,Urdhva Tiryakbhayam, and Anurupye. It has been found that Nikhilam is the most efficient among these. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Hence multiplications in DSP blocks can be performed at faster rate. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering. Digital signal processing (DSP) is the technology that is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Trans forms , etc.With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Hence Vedic mathematics can be aptly employed here to perform multiplication.

Thus, integrating Vedic mathematics for the multiplier design will enhance the speed of multiplication operation. The multiplier architecture is based on Urdhva Tiryagbhyam [4] (vertical and cross-wise algorithm) sutra. An illustration of Urdhva Tiryagbhyam sutra is shown in Figure 1.

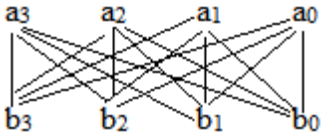

Figure 1. Illustration of Urdhva Tiryagbhyam sutra.

The 4x4 multiplication has been done in a single line in Urdhva Tiryagbhyam sutra [1], whereas in shift and add (conventional) method, four partial products have to be added to get the result. Thus, by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required calculating the final product will be reduced and hence there is a reduction in computational time and increase in speed of the multiplier.

Consider two 4-bit binary numbers a3a2a1a0 and b3b2b1b0. The partial products [5] (P7P6P5P4P3P2P1P0) generated are

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given by the following equations:
i. P0= a0b0
ii. P1= a0b1 + a1b0
iii. P2 = a0b2 + a1b1 + a2b0+ P1
iv. P3= a0b3 + a1b2 + a2b1 + a3b0+ P2
v. P4 = a1b3 + a2b2 + a3b1 + P3
vi. P5 = a1b2 + a2b1 + P4
vii. P6 = a3b3 + P5
viii. P7 = carry of P6 (1)

II. PROPOSED 8X8 MULTIPLIER

The 8-bit multiplier is designed using four 4x4 Vedic multipliers which employ Urdhva Tiryagbhyam sutra and carry skip technique for partial product addition. The output of these Vedic multipliers is added by modifying the logic levels of ripple carry adder. Block diagram of the proposed 8x8 multiplier is illustrated in figure 2.

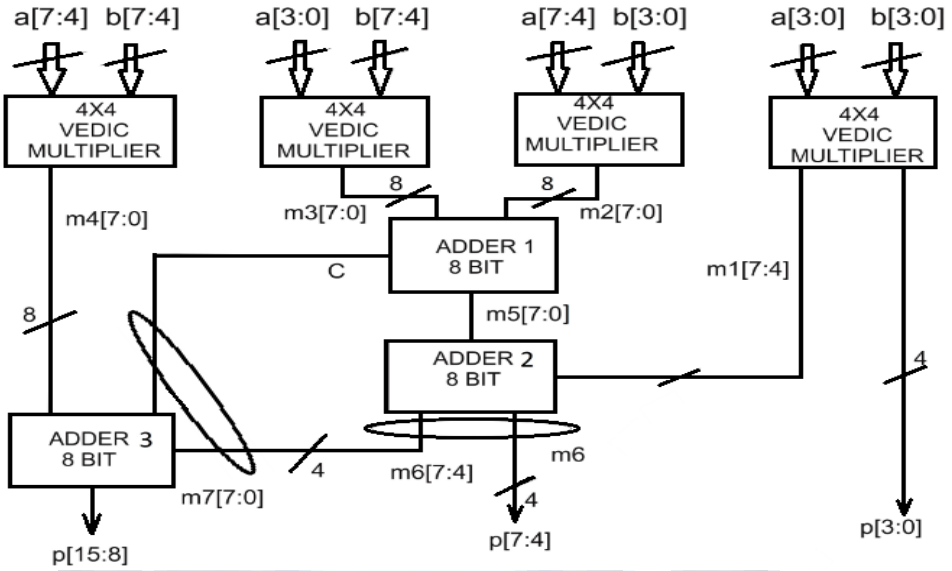

Figure 2. Block diagram of proposed 8x8 multiplier.

The 8-bit input sequence is divided into two 4-bit numbers and given as inputs to the 4-bit multiplier blocks (a[7:4] & b[7:4], a[3:0] & b[7:4], a[7:4] & b[3:0], a[3:0] & b[3:0]). The four multipliers used (in figure 2) are similar and give 8-bit intermediate products which are added using overlapping logic with the help of three modified parallel adders (ADDER-1, ADDER-2 and ADDER-3), explained in subsequent section. The partial products obtained from the four multipliers are demarcated into four regions as in figure 3. The four LSB product bits P[3:0] are directly obtained from one of the multipliers. The output of the second and third multiplier block is added directly using ADDER-1 as the second and third region is overlapping. Then the higher order bit of first multiplier block is added to the overlapping sum using ADDER-2 which gives the product P[7:4]. Finally, MSB bits P[15:8] are obtained by adding the fourth multiplier output to the carry from ADDER-1 (added at the fifth bit position) and higher order bits (acts as lower nibble of addend) of ADDER-3.

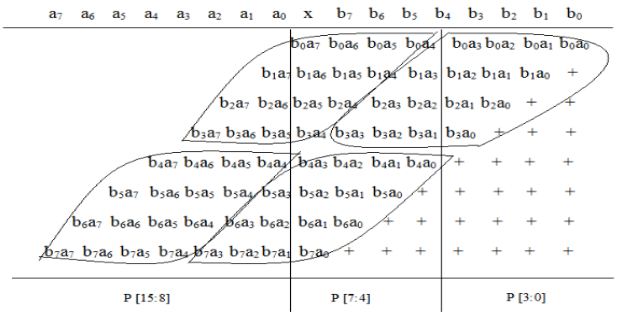

Figure 3. Separation of the partial products

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A. Design of 4x4 Multiplier

The 4-bit Vedic multiplier is designed using Urdhva Tiryagbhyam sutra and carry-skip technique for partial product addition. In a normal Vedic multiplier, the carry from each partial product addition is given to the next partial product bit calculation. In the proposed architecture (Figure 4), the carries are not only rippled to the next partial product bit calculations but also to the subsequent bits using carry skip technique so as to reduce the carry propagation delay.

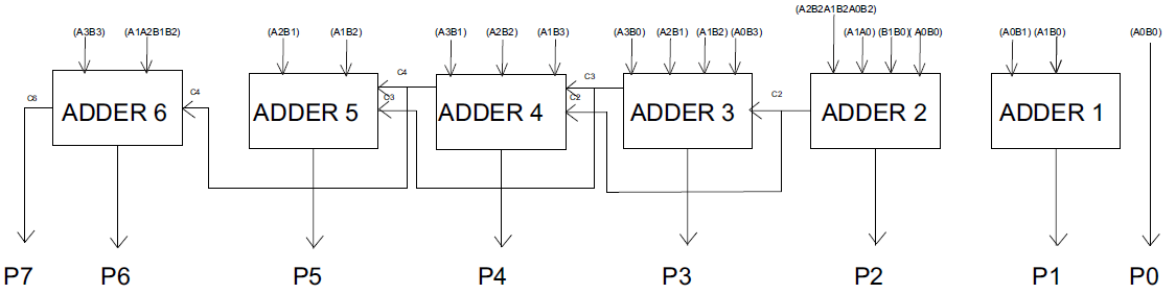

Figure 4. Proposed 4-bit Vedic multiplier using Urdhva Tiryagbhyam sutra and carry-skip technique.

The Vedic multiplier equations given in equation 1 are modified in the proposed multiplier as follows:
i. P0 = a0b0
ii. P1 = a1b0 + a0b1
iii. P2 = a2b0 + a1b1 + a0b2 + a0a1b0b1
iv. P3 = a3b0 + a2b1 + a1b2 + a0b3 + carry from P2
v. P4 = a3b1 + a2b2 + a1b3 + carry from P2 + carry from P3
vi. P5 = a3b2 + a2b3 + carry from P4 + carry from P3
vii. P6 = a3b3 + a1a2b1b2+ carry from P4
viii. P7 = carry from P6 (2)

The products P0, P1, P3 and P7 in equation 2 are same as in equation 1 but the other equations have been modified to incorporate carry skip technique in the adder blocks of figure 2. In P2 a new term a0b0a1b1 is added so that all the four terms are ready for addition at the same time to reduce the delay in waiting for carry from the previous stage. In P4 and P5 the carry from two previous stages are added thus carry propagation time is reduced. For example if all four terms of P2 are 1, the carry is directly transferred to P4. Similarly P6 is modified by adding carry from P4 and term a1a2b1b2.

The gate level description of modified Vedic multiplier is shown in figure 5. The design methodology combines Urdhva Tiryagbhyam sutra [1] of Vedic mathematics with carry skip or carry by pass technique. The figure 5 gives detailed description of how each partial product is obtained in the multiplication process. If any stage produces a two bit carry, then the immediate stage is skipped and the carry is given to the subsequent stages after the immediate stage thus increasing the speed. It uses only half adders and the input bits are added using carry save method.

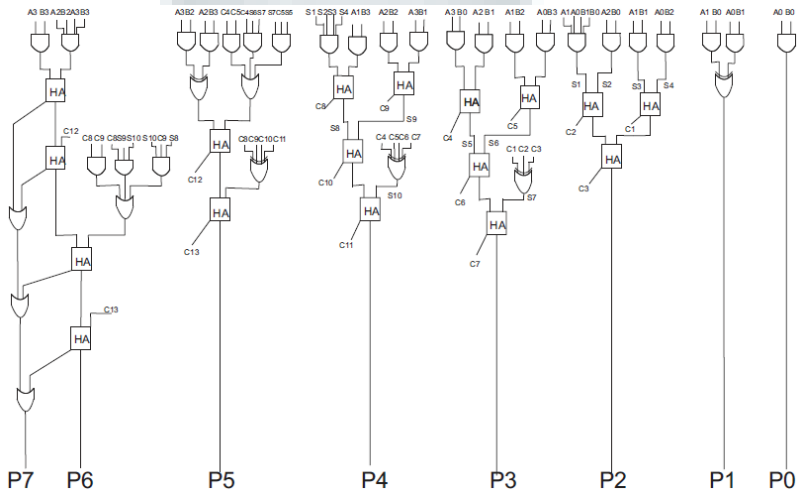

Figure 5. Gate Level description of modified 4-bit multiplier.

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III. ADDERDESIGN

The multiplier in the proposed design uses three adders. The ADDER-1 in figure 6 adds the 8-bit outputs from the second and third multiplier blocks and uses one half adder followed by seven full adders which are connected in ripple carry adder form.

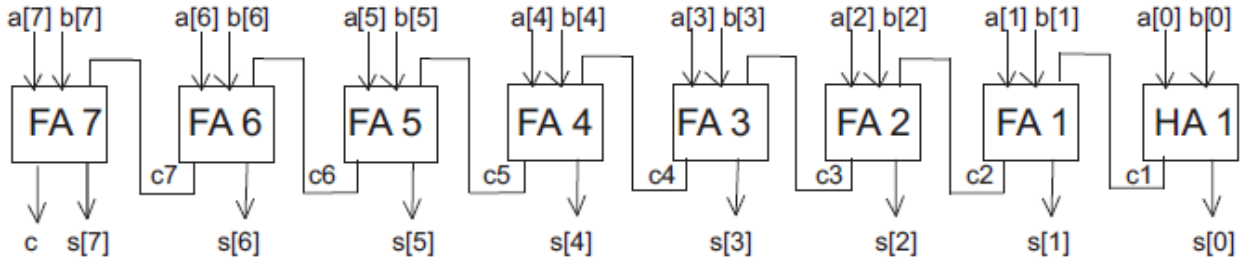

Figure 6. Block Diagram of ADDER1.

The ADDER-2 in figure 7 adds the higher nibble of the first multiplier with the sum output of ADDER-1. It consist of four half adders, three full adders and a XOR gate. The lower nibble of ADDER-2 forms a part of the final product (p [7:4]).

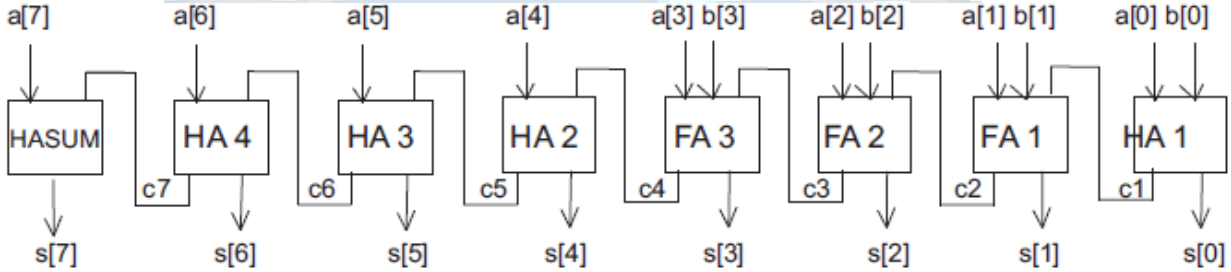

Figure 7. Block Diagram of ADDER-2

The ADDER-3 in figure 8 adds 8-bit word and a 5-bit word. It performs addition on the 8-bit output of the fourth multiplier, the higher nibble of the second adder and carry from the first adder (carry forms the MSB of the augend). The ADDER-3 consists of three half adders, four full adders and a XOR gate. The 8-bit output of the third adder forms the higher byte of the final product. (p[15:8]).

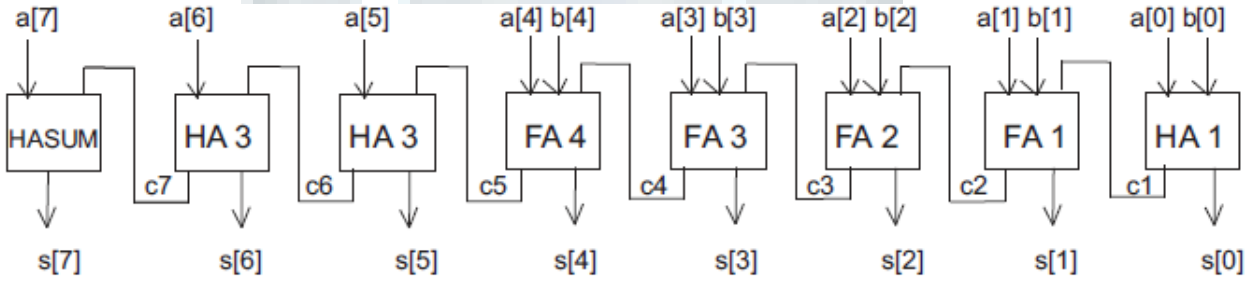

Figure 8. Block Diagram of ADDER-3

IV. RESULT AND DISCUSSION

The proposed 8-bit multiplier is coded in Verilog HDL, simulated using Xilinx ISim simulator, synthesized using Xilinx XST for Spartan 6: xc6slx4-3tqg144 FPGA and verified for possible inputs given below. Inputs are generated using Verilog HDL test bench. The simulation result for 8-bit multiplier is shown in the Figure 9.

CASE - 1: Inputs a = “11111111”, b = “11101101”
Product p = “1110110000010011”
CASE - 2: Inputs a = “10001001”, b = “01001001”
Product p = “0010011100010001”
CASE - 3: Inputs a = “01010110”, b = “01000000”
Product p = “0001010110000000”

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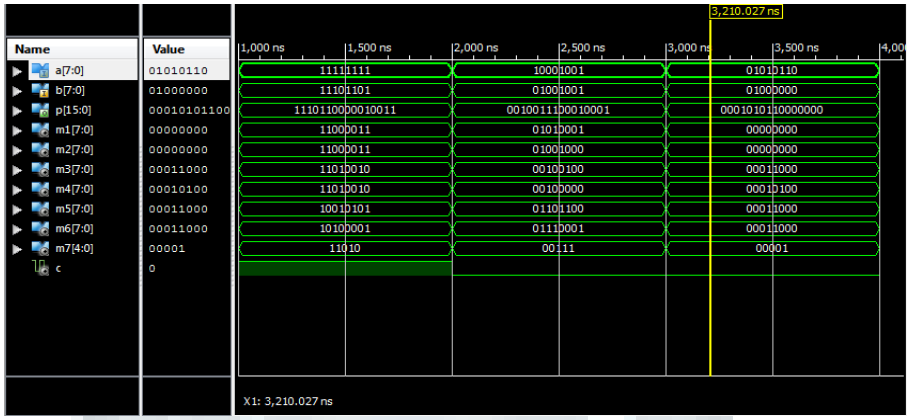

Figure 9. Simulation results for various input combinations

Comparison with Various Architectures

The 8-bit multiplier designed is compared with various architectures in terms of total delay, logic delay, route delay and number of logic levels. The results obtained are tabulated in Table I. From table I, it is evident that there is a reduction in both total delay and logic levels. The routing delay is found to be 9.424 ns, the logic delay is 5.626 ns; thus, giving a total delay of 15.050 ns. The number of logic levels is 11. Thus, it is clear that the proposed design outperforms the other popular multiplier architectures. The proposed architecture can be used to develop a high speed complex number multiplier with reduced delay.

Multiplier Type	Proposed 8-bit multiplier	Normal 8-bit Vedic multiplier	8-bit array multiplier using CSA	8-bit Wallace tree multiplier
Total Delay (ns)	15.050	17.430	17.533	15.969
Logic Delay (ns)	5.626	6.030	6.026	5.823
Route Delay (ns)	9.424	11.400	11.507	10.146
Logic Levels	11	13	13	12

Table I. Comparison between proposed and other architectures.

From table I, it is evident that there is a reduction in both total delay and logic levels. The routing delay is found to be 9.424 ns, the logic delay is 5.626 ns; thus, giving a total delay of 15.050 ns. The number of logic levels is 11. Thus, it is clear that the proposed design outperforms the other popular multiplier architectures. The proposed architecture can be used to develop a high speed complex number multiplier with reduced delay.

V. CONCLUSION

This paper presents a novel way of realizing a high speed multiplier [2] using Urdhva Tiryagbhyam sutra and carry skip addition technique. A 4-bit modified multiplier is designed. The 8-bit multiplier is realized using four 4-bit Vedic multipliers and modified ripple carry adders. Ripple carry adders are modified because not all bits have same weight and hardware can be reduced by reducing the number of full adders used. Though the number of gates used is fairly high, the increase in speed compensates for the increase in area. The proposed 8-bit multiplier gives a total delay of 15.050 ns which is less when compared to the total delay of any other renowned multiplier architecture. Results also indicate a 13.65% increase in the speed when compared to normal Vedic multiplier without carry-skip technique. Our design outshines all other designs.

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