



DESIGN AND IMPLEMENTATION OF ADVANCED BOOTH RECORDER FOR FUSED ADD-MULTIPLY OPERATOR

#1POLAVENI SAGARIKA – Pursuing M.Tech,
#2V.PRAVEEN KUMAR –Assistant Professor, Dept of ECE,

SREE CHAITANYA INSTITUTE OF TECHNOLOGICAL SCIENCES, KARIMNAGAR, T.S., INDIA.

Abstract: This proposed method is purely based on modified recoding techniques for booth recoding in DSP application. The proposed method implements a newly designed recoding technique for modified booth recoding. This technique to implement the direct recoding of the multiplier in its Sum Modified Booth (S-MB) form. The proposed S-MB algorithm is structured, simple and can be easily modified in order to apply either in signed or unsigned numbers, which comprise of odd or even number of bits. Thus Fused Add-Multiply operator is optimized to increase the performance of complex arithmetic operation. It is optimized with three different recoding schemes SMB1,S-MB2, S-MB3. The proposed technique yields considerable reductions in terms of critical delay, hardware complexity and power consumption of the FAM unit. Power consumption has become a critical concern in today's VLSI system design. The growing market for fast floating-point co-processors, digital signal processing chips, and graphics processor has created a demand for high speed, area-efficient multipliers. This paper presents efficient design of multiplier that combines the features of Wallace tree and Modified Booth algorithm, and aimed at reduction of area and improvement in speed. An efficient Verilog HDL code has been written, successfully simulated and synthesized for Xilinx FPGA vertex-6 low power (Xc6vlx75tl-1Lff484) device, using Xilinx 12.2 ISE and XST. The analyses obtained from implementation show that architecture is 41% faster than the Wallace tree architecture with optimal area utilization.

Keywords:- Multiplier, Adder, Modified booth recoding, Wallace tree, Xilinx.

I. INTRODUCTION

Booth recoding is widely used to reduce the number of partial products in multipliers. The benefit is mainly an area reduction in multipliers with medium to large operand widths (8 or 16 bits and higher) due to the massively smaller adder tree, while delays remain roughly in the same range. Different recordings exist resulting in different gate level implementations and performance. In this work the XOR-based implementation gives lowest area and delay numbers in most technologies due to the small selector size and the well-balanced signal paths. An implementation of a radix-4 butterfly has been developed. The number of stages has been reduced. This reduction comes from the fact that, to achieve a throughput comparable to that of radix-2. Therefore, the implementation of the radix-4 butterfly is suitable for high speed applications, since the hardware cost, the power consumption and the latency are reduced. To reduce the number of calculation steps for the partial products, MBA algorithm has been applied mostly where Wallace tree has taken the role of increasing the speed to add the partial products. The straightforward design of the AM unit, by first allocating an adder and then driving its output to the input of a multiplier, increases significantly both area and critical path delay of the circuit. For Booth arrays, typically radix-4, their truncation history followed a similar path to that of the AND arrays, first following truncation [18] and column promotion [19]. Exhaustive simulation of the truncated part of the Booth array was used to design compensation circuitry based upon the conditional exception of the error [20], or in order to construct Karnaugh maps of the ideal correction. Truncated arrays also have been considered for squarers, radix-4 and 16 and Booth squarers, radix-4 and 16 and Booth squarer arrays [21-23]. The structural optimization is performed on the

conventional Wallace tree multiplier, in such a way that the latency of the total circuit reduces considerably. The conventional Wallace tree multiplier architecture [24-25] comprise of an AND array for computing the partial products, a carry save adder for adding the partial products so obtained and a carry propagate adder in the final stage. Recently, the technique of [10] has been used for the design of high performance flexible coprocessor architectures targeting the computationally intensive DSP application [12]. Zimmermann and Tran [11] present an optimized design of [9] which results in improvements in both area and critical path. performance of the MAC operation in terms of area occupation, critical path delay or power consumption. MAC components increase the flexibility of DSP data path synthesis as a large set of arithmetic operations can be efficiently mapped onto them. Except the MAC/MAD operations, many

DSP applications are based on Add-Multiply (AM) operations. The straightforward design of the AM unit, by first allocating an adder and then driving its output to the input of a multiplier, increases significantly both area and critical path delay of the circuit. The proposed system optimize the design of AM operators, by introducing fusion techniques which is based on the direct recoding of the sum of two numbers in its Modified Booth (MB) form. The direct recoding of the sum of two numbers in its MB form leads to a more efficient implementation of the fused Add-Multiply (FAM) unit compared to the conventional one. The Sum-Modified Booth (S-MB) recoding techniques are efficiently used to implement the direct recoding of the sum of two numbers in its MB form. The proposed technique yields considerable reductions in terms of critical delay, hardware complexity and power consumption of the FAM unit.



II. EXISTING SYSTEM

Recent research activities in the field of arithmetic optimization have shown that the design of arithmetic components combining operations which share data, can lead to significant performance improvements. Based on the observation that an addition can often be subsequent to a multiplication (e.g., in symmetric FIR filters). Most digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transform(DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic's determines the execution speed proceedings and performance of the entire calculation. Because the multiplier requires the longest delay among the basic operational blocks in digital system, the critical path is determined by the multiplier, in general. For high-speed multiplication, the modified radix-4 Booth's algorithm (MBA) is commonly used. A signed-bit MB recoder which transforms redundant binary inputs to their MB recoding form. A special expansion of the preprocessing step of the recoder is needed in order to handle operands in carry-save representation . proposes a two-stage recoder which converts a number in carry-save form to its MB representation. The first stage transforms the carry-save form of the input number in to signed-digit form which is then recoded in the second stage so that it matches the form that the MB digits request. Recently, the technique of has been used for the design of high performance flexible coprocessor architectures targeting the computationally intensive DSP applications.

An optimized design of the AM operator [1] is based on the fusion of the adder and the MB encoding unit into a single data path block by direct recoding of the sum $Y=A+B$ to its MB representation. The fused Add-Multiply (FAM) component contains only one adder at the end (final adder of the parallel multiplier). As a result, significant area savings are observed and the critical path delay of the recoding process is reduced. FAM Design is a new technique for direct recoding of two numbers in the MB representation of their sum. FAM design with sum-modified booth (S-MB) recoding technique reduce the number of partial products and increasing speed of calculation. In Existing System the S-MB technique has be implemented by Radix-4. The FAM technique which decreases the critical path delay and reduces area and power consumption.

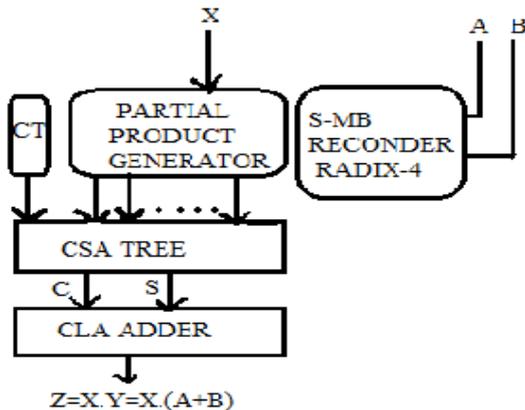


Figure.1. The Architecture of FAM Design by Radix-4.

The S-MB algorithm by radix-4 is structured, simple and can be easily modified in order to be applied either in signed (in 2's complement representation) or unsigned numbers, which comprise of odd or even number of bits.

A.S-MB Recoder Block

The sum to modified booth recoder is embedded with adder and encoder block .It is structured with half adders and full adders where the adder and encoding is done in single structure.This fused block reduces the area of the FAM design.This S-MB Recoder block is implemented by S-MB Recoder technique. The S-MB Recoder technique may be a radix-4 or radix-8. The radix-4 is the existing technique and the proposed technique is radix-8.

B. Modified Booth Encoding (MBE)

Modified Booth (MB) is a prevalent form used in multiplication. It is a redundant signed-digit radix-4 encoding technique. Its main advantage is that it reduces by half the number of partial products in multiplication comparing to any other radix-2 representation. Radix-4 booth encoder performs the processes of encoding the multiplicand based on the multiplier bits. It will compare three bits at a time with overlapping technique .Grouping starts from the LSB and the first block uses the two bits of the multiplier and assume zero as a third bit as shown in the figure 2.

1 1 1 0 0 0 1 1 0

Fig 2. 3 Bit pairing as Booth Recorder.

- Extend the sign bit 1 position if necessary to ensure that n is even.
- Append a 0 to the right of the LSB of the multiplier.
- According to the value of each vector, each Partial Product will be 0, +y, -y, +2y or -2y.

The negative values of y are made by taking the 2's complement. The negative values of y are made by taking the 2's complement and Carry-look-ahead (CLA) fast adders are used for addition . The multiplication of y is done by shifting y by one bit to the left. Thus, in any case, in designing n-bit parallel multipliers, only n/2 partial products are generated.The advantage of this method is the halving of the number of partial products. This is important in circuit design as it relates to the propagation delay in the running of the circuit, and the complexity and power consumption of its implementation. The functional operation of Radix-4 booth encoder is shown in the Table.I. It consists of eight different types of states and during these states we can obtain the outcomes, which are multiplication of multiplicand with 0,-1 and -2 consecutively. Radix-4 Booth algorithm is given in table I.



TABLE I
Booth Recoding Table for Radix-4

Multiplier Bits Block			Recoded 1 bit pair		2 bit Booth	
i+1	i	i-1	i+1	i	Multiplier Value	Partial Product
0	0	0	0	0	0	$M \times 0$
0	0	1	0	-1	+1	$M \times 1$
0	1	0	+1	+1	+1	$M \times 1$
0	1	1	+1	0	+2	$M \times 2$
1	0	0	-1	0	-2	$M \times -2$
1	0	1	-1	-1	-1	$M \times -1$
1	1	0	0	0	-1	$M \times -1$
1	1	1	0	+1	0	$M \times 0$

III. PROPOSED METHOD

In proposed system the S-MB block is implemented by radix-8. The main advantage of radix-8 is that it reduces the number of partial product in multiplication than any other radix-2, radix-4 representation. The S-MB algorithm by radix-8 is implemented for odd and even number of bits.

100100010011

Fig. 4 Bit pairing as Booth Recoder
Radix-8 take quartets of bits instead of triplets.

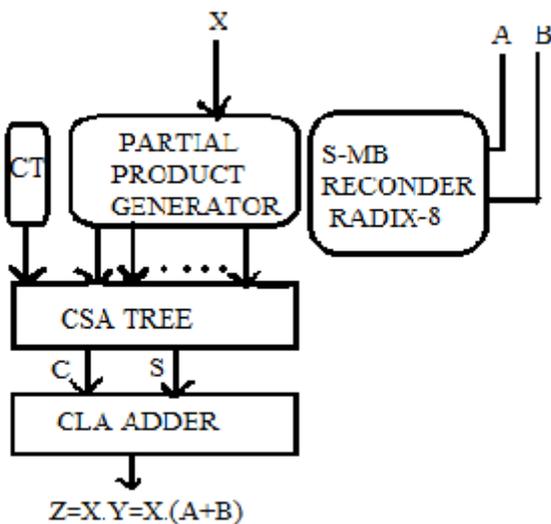


Fig 4. The Architecture of FAM Design by Radix-8.

A. S-MB Recoding Techniques

Both the conventional and signed HAs and FAs is used to design the three new alternative schemes of the S-MB recoding technique by radix-8 Booth encoding. Each of the three schemes can be easily applied in either signed (2's complement representation) or unsigned numbers which consist of odd or even number of bits. Consider that both inputs A and B are in 2's complement form and consist of 2k bits in case of even or 2k+1 bits in case of odd bit-width. Targeting to transform the sum of A and B (Y=A+B) in its MB representation. The three S-MB recoding schemes are:

- S-MB1 Recoding Scheme
- S-MB2 Recoding Scheme
- S-MB3 Recoding Scheme

These S-MB1, S-MB2, S-MB3 Recoding Techniques are implemented by Radix-8 encoding Techniques.

B. Radix-8 Booth Encoding

Booth algorithm (MB) is a prevalent form used in multiplication and it is a powerful algorithm for signed number multiplication. It treats both the positive and negative number uniformly. Its main advantage is that it reduces by half the number of partial products in multiplication comparing to any other radix-4 representation. Radix-8 booth encoder performs the processes of encoding the multiplicand based on the multiplier bits. Radix-8 Booth recoding is the same algorithm as that of Radix-4. Radix-8 take quartets of bits instead of triplets. The number of partial product can be reduces to n/3 by means of Radix-8 booth encoding where n is the number of multiplier bits. Each quartet is coded as a signed digit using Table II.

TABLE II
Booth Recoding Table for Radix-8

Multiplier Bits Radix				Radix-8 Booth Encoding	
Y_{i+2}	Y_{i+1}	Y_i	Y_{i-1}	Multiplier value	Partial Product
0	0	0	0	0	$M \times 0$
0	0	0	1	+1	$M \times +1$
0	0	1	0	+1	$M \times +1$
0	0	1	1	+2	$M \times +2$
0	1	0	0	+2	$M \times +2$
0	1	0	1	+3	$M \times +3$
0	1	1	0	+3	$M \times +3$
0	1	1	1	+4	$M \times +4$
1	0	0	0	-4	$M \times -4$
1	0	0	1	-3	$M \times -3$
1	0	1	0	-3	$M \times -3$
1	0	1	1	-2	$M \times -2$
1	1	0	0	-2	$M \times -2$
1	1	0	1	-1	$M \times -1$
1	1	1	0	-1	$M \times -1$
1	1	1	1	0	$M \times 0$

C. Partial Product Generator

A product formed by multiplying the multiplicand by one digit of the multiplier when the multiplier has more than one digit. Partial products are used as intermediate steps in calculating larger products. Partial product generator is designed to produce the product by multiplying the multiplicand M by 0, 1, -1, 2, -2, -3, -4, 3, 4. For product generator, multiply by zero means the multiplicand is multiplied by "0". Multiply by "1" means the product still remains the same as the multiplicand value. Multiply by "-1" means that the product is the two's complement form of the number. Multiply by "-2" is to shift left one bit the two's complement of the multiplicand value and multiply by "2" means just shift left the multiplicand by one place. Multiply by "-4" is to shift left two bit the two's



complement of the multiplicand value and multiply by “2” means just shift left the multiplicand by two place.

IV. RESULTS AND DISCUSSION

The performance of the three proposed recoding schemes in a fused sum-product operator and implemented them using structural Verilog HDL for both cases of even and odd bit-width of the recoder’s input numbers. We also synthesized all designs at lower frequencies in order to explore how they behave considering different timing is constraints in terms of area, timing and power consumption, we simulated the designs using Modelsim for the same set of pairs of input numbers in 2’s complement representation. The performance of the Fused sum- product designs include the proposed in recoding schemes with respect to the bit width of the input numbers. The lowest area and power values of each clock period are marked.

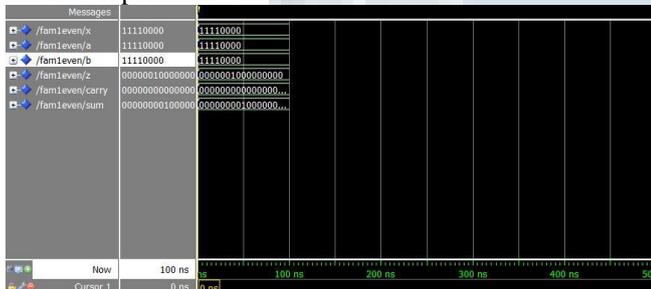


Fig. 5 simulation of odd for s-mb1. A & B can be recorded in a sum-modified booth algorithm. The output of A & B can be partial product to X. Finally Z be the output

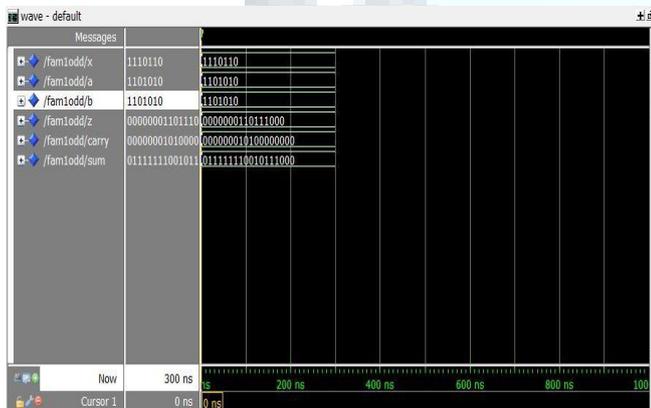


Fig 6 Simulation Of Even for S-Mb1. A & B can be recoded in a sum-modified booth algorithm. The output of A & B can be partial product to X. Finally Z be the output

V. CONCLUSION

The design of sum-product are used to implement the direct recoding of the sum of two numbers in its Modified Booth (MB) form to synthesize each Fused sum-product design at the highest achievable frequency. This paper also synthesized all designs at lower frequencies in order to explore how they behave different timing constraints in terms of area, timing and power consumption. The proposed recoding schemes (S-MB1, S-MB2 and SMB3) achieve area reduction . compare to existing recoders the power has been reduced. The performance of the Fused sum-product designs

that include the proposed recoding schemes is considered with respect to the bit width of the input numbers. The area and power measurements of all Fused sum-product units for different clock periods for even (i.e., 8, 12, 16, 24 and 32 bits) and odd (i.e., 7,11, 15, 23 and 31 bits) bit-width of the recoder. The Fused Add-Multiply operator is optimized to increase the performance of complex arithmetic operation. It is optimized with three different recoding schemes S-MB1, SMB2, S-MB3. This proposed system implement the modified booth recoding techniques in radix-8 to achieve the power consumption. The proposed technique yields considerable reductions in terms of critical delay, hardware complexity and power consumption of the FAM unit.

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AUTHOR'S PROFILE:



[1]. **POLAVENI SAGARIKA**
Pursuing M.Tech, Dept of ECE,
SREE CHAITANYA INSTITUTE
OF TECHNOLOGICAL SCINCES,
KARIMNAGAR, T.S., INDIA.



[2]. **V.PRAVEEN KUMAR** working
as Assistant Professor , Dept of ECE,
SREE CHAITANYA INSTITUTE
OF TECHNOLOGICAL SCINCES,
KARIMNAGAR, T.S., INDIA.

