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AN IMPROVED HIGH-POWER AC/DC CONVERTER FOR DDISTRIBUTED POWER GENERATORS

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ABSTRACT: Single-Stage transformer less AC/DC converter received much attention in the universal line application. In this work, the design and development of a high step down transformer less single stage single switch ac/dc converter suitable for universal line applications (90–270 Vrms) is discussed. Here for experimental set up we obtain 19V output by giving 100V as input. Important feature of this topology is that it uses Direct power transfer scheme. The advantage of this topology is that it uses single switch for power factor correction and voltage regulation. The converter utilizes a buck converter as a PFC cell and buck-boost converter as a DC/DC cell. The absence of transformer reduces the component count, size and cost of the converter. This paper introduces a new transformer less dc–ac converter with the feature that it produces an instantaneous output voltage higher or lower than the input dc voltage. The topology consists of two switching cells, well known dynamic response, does not have transformer or power conversion stage that saves us mass, losses, and volume of a transformer. The merits of step up/step down dc-ac converter includes operational reliability, reduced size of components and there by acquiring less mass for the whole converter. The advantages of buck-boost dc-ac converter when switching cells are used instead of a transformer, is also introduced. Current control takes the advantage of circuit protection from disturbance (fault). This technique can provide fast dynamic response, robust Performance. The current control of step up/step down dc-ac converter is easy to implement and provides high accuracy.

Key Words- *AC/DC, PFC, Integrated buck-buck- boost converter, THD.*

I. INTRODUCTION

AC/DC converters are mainly single stage and two stage converters. An ac to dc converter is an integral part of any power supply unit used in all the electronic equipments .Also, it is used as an interface between utility and most of the power electronic equipments. These electronic equipments form a major part of load on the utility. Generally, to convert line frequency ac to dc, a line frequency diode bridge rectifier is used. To reduce the ripple in the dc output voltage, a large filter capacitor is used at the rectifier output. But due to this large capacitor, the current drawn by this converter is peaky in nature. This input current is rich in low order harmonics. Also, as power electronics equipments are increasingly being used in power conversion, they inject low order harmonics into the utility. Due to the presence of these harmonics, the total harmonic distortion is high and the input power factor is poor. Due to problems associated with low power factor and harmonics, utilities will enforce harmonic standards and guidelines which will limit the amount of current distortion allowed into the utility and thus the simple diode rectifiers may not in use. So, there is a need to achieve rectification at close to unity power factor and low input current distortion. Initially, power factor correction schemes have been implemented mainly for heavy industrial loads like induction motors, induction heating furnaces etc., which forms a major part of lagging power factor load. However, the trend is changing as electronic equipments are increasingly being used in everyday life nowadays. Hence, PFC is becoming an important aspect even for low power application electronic equipments. As for single-stage approach (SS), it is a very attractive solution in low power application as two power stages (PFC cell and DC-DC cell) are combined in sharing common switching devices, storage elements and control loop leading to reduced size and cost of converter, also enhancing conversion efficiency. Lately, there were numerous of single stage circuits reported [2-7]. For the sake of circuit simplicity, most PFC cells in SS AC/DC converter are a boost cell for which the output voltage is always greater than the input voltage. At high line application, therefore, this output voltage usually exceeds 450V causing high voltage stress on bulk capacitor and switching devices. It has been reported that this intermediate bus voltage can easily exceed 1000V [3],[4],[7] leading to very limited and costly selection of switching devices and storage capacitor. A single stage approach combines the PFC stage and DC-DC converters to provide a less complex and compact solution. A single power stage circuit is formed by integrating a boost PFC converter with a two-switch clamped flyback isolated converter [5].The current stress of

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the main power switch is reduced due to separated conduction period of the two source currents flowing through the power switch. In this paper, an integrated buck-buck-boost (IBuBuBo) converter with low output voltage is proposed. The converter formed by two converters namely, abuck converter as a PFC cell and a buck-boost converter as a DC/DC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. So a transformer is not needed to obtain the low output voltage. Thus the converter is able to achieve:

1.Low intermediate bus and output voltages in the absence of transformer

2. Simple control structure with a single-switch

3. Positive output voltage

4. High conversion efficiency due to part of input power is processed once and

5. Input surge current protection because of series connection of input source and switch.

Buck-Buck-Boost (BuBuBo) converter circuit configuration and principle of operation is presented in Section II. Operation principle of controller circuit is presented in section III. Simulation result of buck buck-boost converter is given in section IV. Finally conclusion is stated in section V.

The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e., < 10%. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. In this paper, an integrated buck–buck–boost converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell.

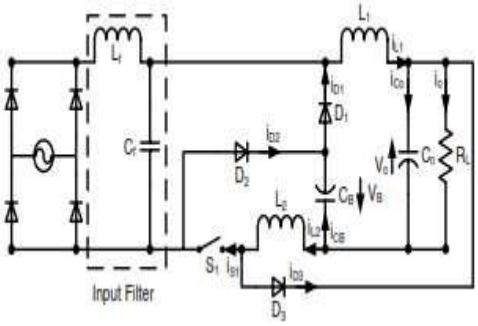

Fig 1: Proposed dc/dc Converter

The figure 1 shows the proposed converter, which consists of the merging of a buck PFC cell (L1, S1, D1, Co, and CB) and a buck–boost dc/dc cell (L2, S1, D2, Co, and Cb) is shown. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there is no currents in both inductors L1 and L2at the beginning of each switching cycle t0. Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

II. OPERATION PRINCIPLE AND CONTROL OF CONVERTER

Transformer less buck-boost inverter is formed by connecting two switching cells. Circuit diagram of the converter is shown in Fig.2. Note that by referring to Fig.1, This structure consists of an input voltage source Vi, a high frequency filter formed by Lf and Cf, a load resistance R0, and two switching cells, whose elements are S1, D1, C1, S2, D2, and L1 and S3, D3, C2, S4, D4, and L2, respectively. When S1, S4 are turned on then L1 starts charging, L2 starts discharging, C2 starts charging, C1 starts discharging. When S2, S3 are turned on L1 starts discharging, C1 starts charging , L2 starts charging , C2 starts discharging.

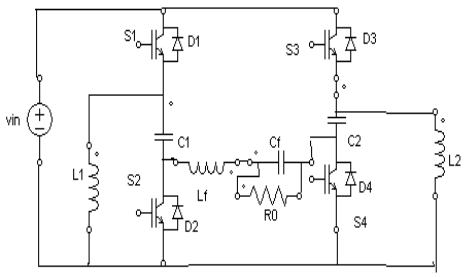

Fig.2. Transformer less buck-boost inverter

III. CURRENT CONTROL

In this paper, a current control method is used for controlling the transformer less buck-boost dc-ac converter. When a low impedance fault is applied to the network, the inverter output voltage will reduce. Then the outer voltage controller will increase the current reference to the inner controller in an attempt to maintain the system voltage. If the increase in current reference is above the maximum current which is allowed for the inverter. Then this current control will activate. This paper discusses a new control technique. This control has two control loops an outer voltage control loop and an inner current control loop. The output of the voltage control loop is the input of the current control loop. An advantage of this approach is that it can be adopted to control both single and three phase micro grids. In the Inner current control loop, the measured inverter current i o (t) is compared with the set value i L∗ (t) of this current. Then the current error is given to a proportional-integral (PI) controller. It is an excellent method to eliminate the disturbance (fault), as well as voltage regulation. The output current has sensed. A reference current (desired current) has to be provided. If there is any overloading condition occurs then the increasing output current is controlled by using this current control technique. Then the

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resultant is given to a linearization function for maintaining the duty ratio. According to the duty ratio the resulting switching signal is given to the gates of the switches S1-S4. Thus by using this technique the over current through the circuit can be eliminated and thereby ensured safety. In order to illustrate the equivalent circuits of the system, two cases were chosen. The first refers to the system operation with a duty cycle higher than 0.5, as shown in Fig. 2, and the second the system operates with a duty cycle lower than 0.5, as illustrated in Fig.3.

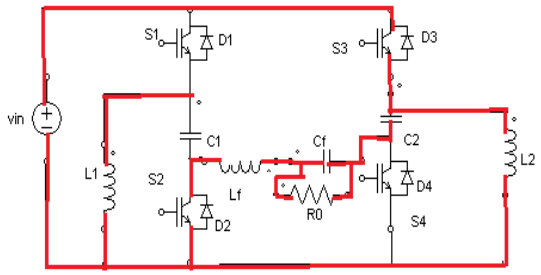

Fig 3. Equivalent circuit for duty cycle higher than 0.5

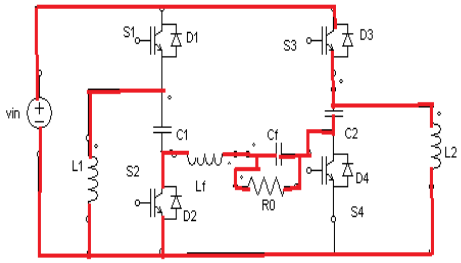

Fig.3. Equivalent circuits for duty cycle lower than 0.5

III. UNDER LIGHT LOAD

Switching loss of power semiconductors is the major cause of low efficiency of single-stage PFC converters under a light-load condition. Due to the dead angle of the input current of the buck PFC cell .It is possible to use this duration to turn OFF the PFC cell to reduce the switching loss of power semiconductors and the conduction loss of passive devices. next section hence explores the possibility of reducing the switching loss by different PWM patterns, while maintaining output voltage (Voregulation and dc-bus voltage (VB) control. Note that it is common in single-stage PFC converters that the bus voltage cannot be regulated but only be controlled within a certain range due to the lack of an extra control device in the simplified converter structure; the power MOSFET can achieve only 1-D control which is the output voltage regulation. Here introduces a possible approach to turning OFF the PFC stage in single-switch S2PFC converters similar to that in the two-stage approach in [1] . The idea takes the advantages of varying the input voltage and dead angle of input current characteristic of the ac/dc converter. The buck or buck derived PFC converter inherently has such characteristic as there are times during a line cycle when the input voltage is smaller than the output voltage and the PFC stage is effectively turned OFF.

IV. OPERATION PRINCIPLE OF CONTROLLER CIRCUIT

Here uses a concept similar to burst mode control [1],[2]. But instead of having a random pattern of pulses, the proposed light-load power management has deterministic patterns of pulses as described as follows. There are four distinctive PWM patterns to operate the single-stage buck-derived PFC converters under a light-load condition. In all cases, the output voltage is regulated by a voltage-mode controller

1. The first scheme (M1) does not use any specific switching pattern. The converter operates at fixed switching frequency and the duty cycle reduces when the load decreases. This scheme is used as a reference for comparison of the proposed power management
schemes (M2 toM4).
2. The second scheme (M2) operates the converter in the zero crossing region of rectified input voltage where the buck PFC cell is inactive (i.e., Mode A). Note that the duration of Mode A is defined by the voltage conversion ratio and is given by arc sin([Vo +VB] =Vpk) according to Fig.2(b) . However, if operating in Mode A only, the dc-bus voltage will decrease to zero gradually as the charge is taken away from the bus capacitor by owing into the buck PFC cell in order to charge the bus capacitor. Therefore, in order to control the bus voltage, the converter will continue to operate and enter Mode B for a short duration so that the buck PFC cell is active. Hence, the bus capacitor can be recharged to maintain its voltage, but at a lower level.
3. The third scheme (M3) operates the converter around the peak input voltage only. Both buck PFC cell and buck boost dc/dc cell are in active states (i.e.,ModeB). Apart from the output regulation, with this method, the dc-bus voltage is somehow controlled as charging and discharging of the bus capacitor occur simultaneously.
4. The fourth scheme (M4) combines the two schemes above; the converter operates at both the zero crossing and peak input voltage regions.

Unlike scheme M2, however, the converter will not operate just beyond the dead angle of input current except for the region around the peak input voltage duration. This method also allows for bus-voltage control and output voltage regulation. The schemes M2M4 define when the converter operates to generate the burst mode patterns. For every burst duration, fixed frequency PWM pulses are used. Practical implementation a logic circuit, as shown in Fig. 4,

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is added to the PWM controller to implement the above three light load power management schemes.

The truth table of the logic circuit is shown in Fig. 4, where X denotes a don't-care option and C1 and C2 denote binary control variables. The light load operations (M2 to M4) will be enabled once RL det is at level high. The signal RL det is generated from the current sensing amplifier and the comparator as shown in Fig. 1. The output load current of RL is sensed via Rs. Once the current in Rs is below a pre-determined level (in this example was equivalent to 3W of output power), RL det will set to high and enable M2 to M4 light load operation schemes. The full logic function of the proposed three light load power management schemes can be summarized by the following Boolean equality:

ENB = RL det + RL det(VB det · VP det + VZ det) (1) where ENB determines when the PWM signal will be sent to the gate of MOSFET, VB det will go high when the bus voltage is lower than the pre-defined level, VP det will go high when peak input voltage is close, and VZ det will go high when the zero crossing region is near.

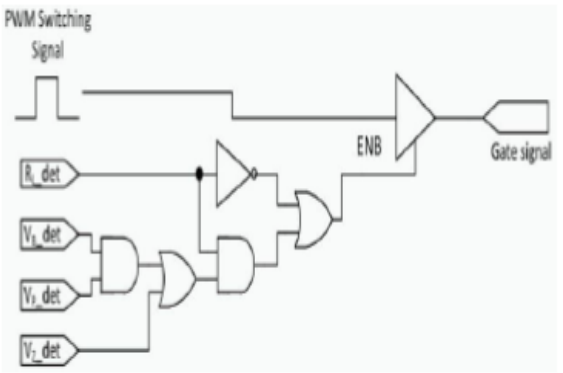


Fig.4: Logic circuit

V. ANALYSIS AND SIMULATION RESULTS

The performance of the proposed circuit is verified by using MATLAB/ Simulink. To achieve high performance of the converter for universal line operation in terms of low bus voltage (< 150V) and high power factor , the inductance ratio has to be optimized. The lower the bus voltage of the converter, lower voltage rating capacitor (150 V) can be used.

Simulation results

1. output power: 100 W
2. output voltage: 19 Vdc
3. power factor: > 96%
4. intermediate bus voltage: < 150V
5. line input voltage: 90–270 Vrms/50 Hz
6. switching frequency (fs): 20 kHz
7. modulation index =0.4

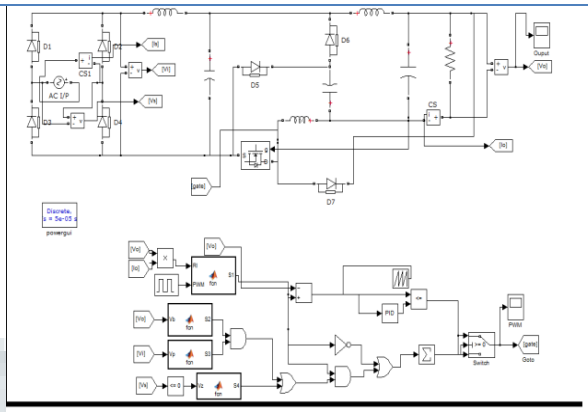
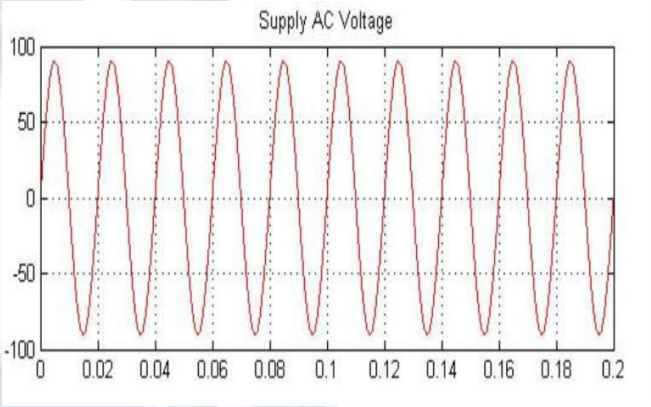
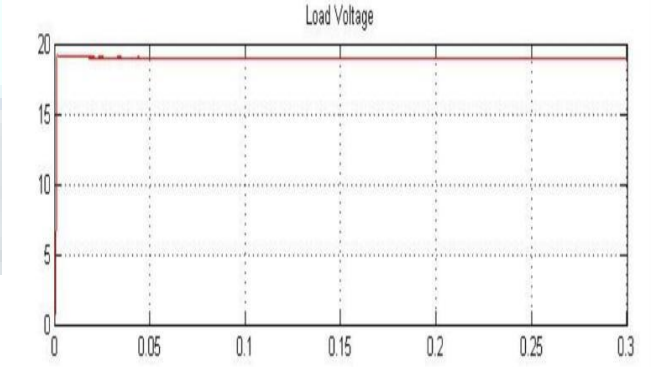


Fig 5:Simulation Diagram of Integrated Buck-Buck-Boost Converter.



(a)



(b)

Fig 6: (a) Input Voltage bB) Output Voltage

VI. CONCLUSION

New transformer less dc-ac converter based on buck-boost topology with two switching cells is presented in this paper. The advantages of step up/step down dc-ac converter includes system reliability, reduction of size of components and there by acquiring less mass for the whole converter. This dc-ac converter operates with the step-up/step-down feature without transformer. This peculiarity is provided by using two switching cells including two switches, diodes, one inductor, and capacitor on each leg of the inverter. The main advantage of the new inverter

topology is that it generates an ac output voltage larger than the dc input one, based on the duty cycle.

it is able to achieve bus voltage below 150V at all input and output conditions. So the converter able to achieve less bus voltage and output voltage without using any resonant converters, high step transformers etc. Thus unlike all the existing converters, Buck-Buck-Boost converters can reduce the component count and complexity in control. Reduced bus voltage reduces ,voltage rating of intermediate capacitor. By using Buck-Buck-Boost converter, it is able to achieve a power factor around 0.97.Thus the converter can meet IEC 61000-3-2 standard.

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