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CASCADED MULTI LEVEL INVERTER BASED FOR HIGH-POWER ACTIVE POWER FILTERS

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ABSTRACT: Multilevel inverters have been attracting in favor of academia as well as industry in the recent decade for high-power and medium-voltage energy control. In addition, they can synthesize switched waveforms with lower levels of harmonic distortion than an equivalently rated two-level converter. The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. This paper presents the most important topologies like diode-clamped inverter (neutral- point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel with separate dc sources. The new topology produces a significant reduction in the number of power devices and capacitors required to implement a multilevel output. This topology requires fewer components compared to existing inverters (particularly in higher levels) and requires fewer carrier signals and gate drives. A nine level PWM inverter configuration with DC sources are verified through MATLAB/SIMULINK software. Furthermore, an experimental prototype of a nine level inverter for both cascade and RV inverter has been implemented ant total harmonic distortion (THD) is calculated using MATLAB/SIMULINK software. Result have been compared and validated for the same.

Keywords: *Diode Clamped Inverter, Capacitor Clamped Inverter, Cascade H-Bridge Inverter, Modulation Technique.*

I. INTRODUCTION

Multilevel power conversion has been extensively researched in the past few years for high power applications [1], [2]. Many topologies have been introduced for utility and drive applications. The two level inverters require high switching frequency with various PWM strategies to get quality output which leads to high switching losses. To overcome these problems multi level inverters (MLIs) are introduced. It uses higher number of semiconductor switches to perform the power conversion in small voltage steps. The advantages of MLIs are improvement in Staircase waveform quality, reduction in Common-mode (CM) Voltage, less input current distortion [3]. MLI are extensively being used in drives, PV systems, HEV systems, automotive applications [4-8].The various topologies of MLI are Cascade inverter, Neutral-point clamped (NPC) inverter, and Flying capacitor inverter. As the level increases, NPC require many clamping diodes, control of real power flow becomes difficult [13]. In Flying capacitor inverter as the level increases, number of storage capacitors also increases hence becomes bulky and costly; the switching losses are also more [14]. The cascaded multilevel inverter has more advantages than other two topologies [9], [10], since it does not require any balancing capacitors and diodes. Cascaded inverter needs separate DC sources for each H-Bridge, hence there is no voltage balancing problem, but isolated DC sources are not readily available, this could be main drawback of this topology[15][16]. Cascaded topology requires more switches. These disadvantages are overcome by a new topology known as Reversing Voltage Component [10].

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly.As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations Subsequently, several multilevel converter topologies have been developed. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. The term multilevel began with the three level converter. The advantages of three-level Inverter topology over conventional two-level topology are:

- The voltage across the switches is only one half of the DC source voltage;
- The switching frequency can be reduced for the same switching losses;
- The higher output current harmonics are reduced by the same switching frequency.

Plentiful multilevel converter topologies have been proposed during the last two decades.

Moreover, three different major multilevel converter structures have been reported in the literature: cascaded H-bridges converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors

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(capacitor clamped). Moreover, abundant modulation techniques have been developed.

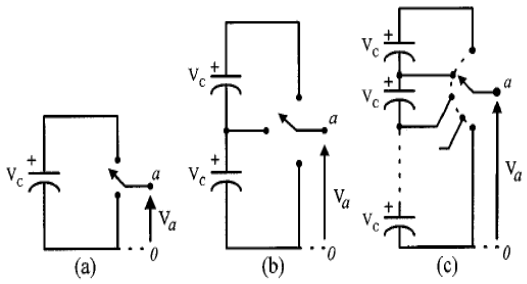

Figure.1: One Phase Leg Of An Inverter With (A) Two Levels, (B) Three Levels, And (C) N Levels.

Figure.1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor [see Fig. 1(a)], while the three-level inverter generates three voltages, and so on. The most attractive features of multilevel inverters are as follows.

1. They can generate output voltages with extremely low distortion and lower .
2. They draw input current with very low distortion.
3. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
4. They can operate with a lower switching frequency.

The conventional topologies of multilevel inverter fundamentally are diode clasped and capacitor-cinched sort . The for-mere utilizes diodes to clasp the voltage level, and the recent uses extra capacitors to clip the voltage. The higher number of voltage levels can then be acquired; on the other hand, the circuit be-comes to a great degree intricate in these two topologies. An alternate sort of multilevel inverter is fell H-Bridge built by the arrangement association of H-Bridges. The fundamental circuit is like the established H span DC–DC converter. The fell structure expands the framework dependability due to the same circuit cell, control structure and balance. How-ever, the disservices went up against by fell structure are more switches and various inputs. With a specific end goal to expand two voltage levels in staircase yield, a H-Bridge built by four force switches and an individual info are required. The-cortically, fell H-Bridge can get staircase yield with any number of voltage levels, yet it is improper to the applications of expense sparing and information confinement.

Various studies have been performed to expand the quantity of voltage levels. An super capacitor (SC) based multilevel circuit can adequately expand the quantity of voltage levels. Notwithstanding, the control methodology is perplexing, and EMI issue gets to be more regrettable because of the intermittent data current. A solitary stage five-level pulse width-tweaked (PWM) inverter is constituted by a full scaffold of diodes, two capacitors and a switch. Be that as it may, it just furnishes yield with five voltage levels, and higher number of voltage levels is restricted by circuit structure [16].

A SC-based fell inverter was given SC frontend and full extension backend. Notwithstanding, both entangled control and expanded parts utmost its application [17]. The further study was introduced utilizing arrangement/parallel transformation of SC. Then again, it is improper to the applications with HF out-put due to multicarrier PWM (MPWM). On the off chance that yield recurrence is around 20 kHz, the bearer recurrence achieves a few megahertz. To be specific, the transporter recurrence in MPWM is handfuls times of the yield recurrence.

Since the bearer frequency decides the exchanging recurrence, a high exchanging misfortune is certain for the purpose of high-recurrence yield. A help multilevel inverter situated in fractional charging of SC can expand the quantity of voltage levels hypothetically. In any case, the con-troll system is muddled to actualize incomplete charging [20]. Along these lines, it is a testing errand to present a SC-based multi-level inverter with high-recurrence yield, low yield harmonics, and high transformation productivity. Taking into account the study circumstance previously stated, a novel multi-level inverter and straightforward tweak methodology are displayed to serve as HF force source. Whatever is left of this paper is sorted out as takes after.

II. BASIC OF CASCADED MULTILEVEL INVERTER

A. Topology of the Inverter

Cascaded multilevel inverter is one of the most important topology in the family of multilevel inverters. Multilevel inverters do not need a coupling transformer to interface it with high power system. A five level cascaded H-bridge inverter at the high voltage level has been considered and is operated at a carrier frequency of 3 KHz. The system configuration is shown in Figure 2.

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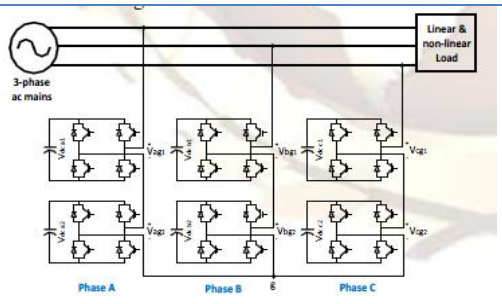

Fig. 2. Cascaded Multilevel Inverter

The cascaded multilevel inverter used here composed of six H-bridges and six dc capacitors. It is connected to the power system in parallel. The number of output phase voltage levels in a cascaded inverter is given as , where s is the number of separate dc sources and m is the inverter level. To obtain 5-level output, two Hbridges are used per phase as shown in Fig.1. If the dc voltage of each cell is set to the same value (Vdca1 = Vdca2 = E), then the resulting inverter can operate with five output voltage levels. Table I. shows the zero and positive voltage levels obtainable from this inverter as well as the voltage levels from the individual H-bridge cells [13].

Table I. output voltage of inverter for phase a

$V_{ag} = V_{ag1} + V_{ag2}$	V_{ag1}	V_{ag2}
0	E	-E
	0	0
	-E	E
E	E	0
	0	E
2E	E	E

B. Modulation

The modulation technique used is based on PSCPWM strategy, In the phase shifted multicarrier modulation, all triangular carriers have same peak to peak amplitude and the same frequency but there is a phase shift between any two adjacent carrier waves of magnitude given by Where *m* is the voltage levels of MLI. Gate signals are generated by comparing the modulating wave with the carrier waves. In this PWM method the equivalent switching frequency of the whole converter is (m-1)times as the each power device switching frequency. This means PSCPWM can achieve a high equivalent switching frequency effect at very low real device switching frequency which is most useful in high power applications [13]. The carrier 1 and carrier 2 are used to generate gating for the upper switches in left legs of power cells H1 and H2 in Fig. 1 respectively. The carrier 1 and carrier 2 are two triangular carrier waves shifted by 90° from each other. The inverted signals are used for upper switches in the right legs. The gate signals for all lower switches operate in a complementary manner with respect to their corresponding upper switches.

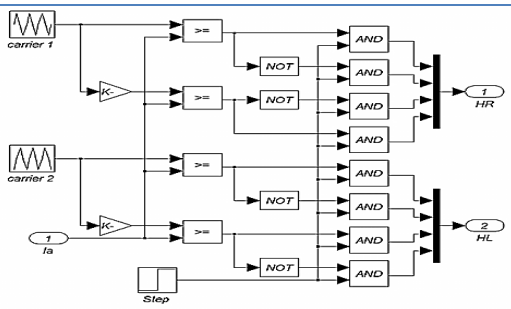

Fig 3. Gating Signal Generation by PSCPWM

Fig. 2 gives the block diagram to generate the gating signals, where modulating signal is MLI reference current and is compared with carrier 1 and

2. The advantage of PSCPWM that the semiconductor device can be used at comparatively low switching frequency so that switching loss is reduced greatly [13],[14].

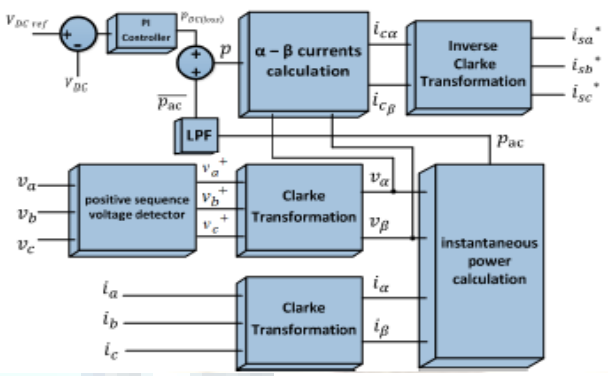

Fig 4. Control block diagram for reference current generation

III. CLASSIFICATION OF CONTROL STRATEGIES

The main aim of the modulation strategy of multilevel inverters is to synthesize the output voltage as close as possible to the sinusoidal waveform. Many modulation techniques have been developed for harmonic reduction and switching loss minimization. The modulation methods used in multilevel inverters can be classified according to switching frequency, as shown in Figure.5.Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is the SVM strategy, which has been used in three-level inverters.

Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination and the space-vector control (SVC).

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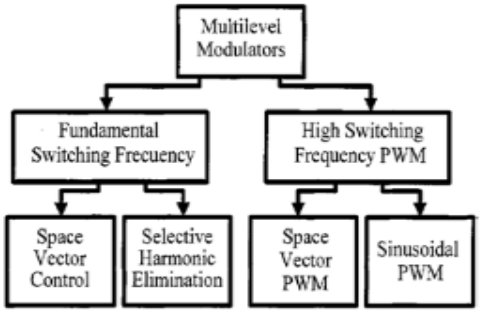

Figure.5:Classification Of Multilevel Modulation Methods.

IV.SPACE VECTOR MODULATION

The basic idea of voltage space vector modulation is to control the inverter output voltages so that their Parks representation will be approximately equals the reference voltage vector. In the case of two level inverter, the output of each phase will be either +Vdc/2 or - Vd&2.The SVM technique can be easily extended to all multilevel inverters. Figure.7 shows space vectors for the traditional two-, three-, and five-level inverters. These vector dia-grams are universal regardless of the type of multilevel inverter. In other words, Figure.7(c) is valid for five-level diode-clamped, capacitor-clamped, or cascaded inverter. The adjacent three vectors can synthesize a desired voltage vector by computing the duty cycle(Tj, T_{j+1} and T_{j+2}) for each vector.

$$V^* = (TjVj + Tj+1Vj+1 + Tj+2Vj+2)/T$$

Space-vector PWM methods generally have the following features: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high-voltage high-power applications. As the number of levels increases, redundant switching states and the complexity of selecting switching states increase dramatically. Some authors have used decomposition of the five level space-vector diagram into two three-level space-vector diagrams with a phase shift to minimize ripples and simplify control.

V.MULTILEVEL SINUSOIDAL PWM

The control principle of the SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. For a m-level inverter, (m-1) triangular carriers are needed. The carriers have the same frequency fc and the same peak-to-peak amplitude AC. The modulating signal is a sinusoid of frequency fm and amplitude Am. At every instant, each carrier is compared with the modulating signal. Each comparison switches the switch "on" if the modulating signal is greater than the triangular carrier assigned to that switch. The main parameters of the modulation process are:

• The frequency ratio k=fc/fm, where fc is the frequency of the carriers, and fm is the frequency of the modulating signal.

• The modulation index M=Am / (m *Ac), where Am is the amplitude of the modulating signal, A, is the peak-to-peak amplitude of the carriers, and m'= (m- 1)/2, where m is the number of level (which is odd).

Figure.6 shows the typical voltage generated by one cell for the inverter by comparing a sinusoidal reference with a triangular carrier signal. A number of –cascaded cells in one phase with their carriers shifted by an angle and using the same control voltage produce a load voltage with the smallest distortion.

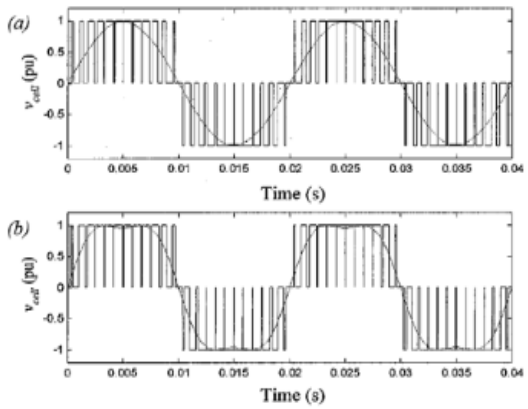

Figure.6: Inverter Cell Voltages. (A) Output Voltage And Reference With SPWM.(B) Output Voltage And Reference With Injection Of Sinusoidal Third Harmonic.

VI.SPACE VECTOR CONTROL

José Rodríguez, et al. [79], addressed a switching strategy for multilevel cascade inverters, based on the space-vector theory. The proposed switching strategy generates a voltage vector with very low harmonic distortion and reduced switching frequency. Anandarup Das, et al. [80], used a new PWM technique for induction motor drives involving six concentric dodecagonal space vector structures are proposed. Liliang Gao, et al. [81], suggested a novel space vector modulation (SVM) technique for a three-level five-phase inverter is described based on an optimized five vectors concept. José Rodríguez, et al. [82], introduced a switching strategy for multilevel cascade inverters, based on the space-vector theory. The proposed high-performance strategy generates a voltage vector across the load with minimum error with respect to the sinusoidal reference.

V. CONCLUSION

In this paper cascaded H-bridge multilevel inverter based APF is implemented in distribution system. This eliminates need of high cost transformer with MLI in high voltage systems. Cascade type inverter has certain advantages as compared with other types. Positive sequence

voltage detector and instantaneous real-power theory is used to generate reference currents of APF.

Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring. This paper cannot cover or reference all the related work, but the fundamental principle of different multilevel inverters has been introduced systematically. Authors strongly believe that this survey article will be very much useful to the researchers for finding out the relevant references as well as the previous work done in the field of multilevel inverter topologies and their modulation technique.

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