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DESIGN AND IMPLEMENTATION OF TRUNCATED MULTIPLIER IN FIR FILTER

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ABSTRACT— Low-cost finite impulse response (FIR) designs are presented using the concept of faithfully rounded truncated multiplier. This multiplier design is usually considered where the maximum absolute error is no more than 1 unit of least position. And also this truncated multipliers offer significant improvement in area, delay and power. The proposed method jointly consider the deletion, reduction, truncation and rounding of partial product bits in order to minimize the number of full adders and half adders during tree reduction. In addition, the truncated multiplier design also has smaller delay due to the smaller bit width in the final carry-propagate adder. In previous papers truncation error is reduced by adding error compensation circuits in fixed width multiplier to get a précised output. But here, there is no need of error compensation circuits and the final output will be précised. The proposed filter using truncated multiplier will be designed using Verilog HDL and synthesis using ISE Simulator (ISIM) and simulate it using MODELSIM ALTERA6.4a (Quartus II 9.2i).It achieves best area and power result when compared with previous FIR design approaches.

Keywords*— low power and area truncated multiplier, DSP,VLSI design, FIR filter Design, partial products.*

I.INTRODUCTION

Multiplication of two numbers generates a product with twice the original bit width. It is usually desirable to truncate the product bits to the required precision to reduce area and cost, leading to the design of truncated multipliers or fixed-width multipliers.Fixed-width multipliers,a subset of truncated multipliers, compute only n most significant bits (MSBs) of the 2n-bit product for n × n multiplication and use extra correction/compensation circuits to reduce truncation errors. There are, in general two truncated multiplier design methods, namely constant and variable corrections, depending on how to compensate the error introduced due to the elimination of the least significant partial product (PP) bits. In some applications like the design of FIR filter in digital Signal processing (DSP) we need truncated multipliers with accuracy of faithful rounding which means that the maximum absolute error after truncation is less than 1 unit of least position (ulp). In these applications, we need to control the computational accuracy of every individual hardware R. Muthammal is Associate Professor, Department of Electronics and Communication Engg, GKM College OfEngg and Technology, Chennai, Tamilnadu, India(email: muthammalr@gmail.com) S. Sandhya is PG Scholar- M.E (DSP) Department of Electronics and Communication Engg, GKM College OfEngg and Technology, Chennai, Tamilnadu, India (email: sandhyaselvam73@gmail.com) component, including multipliers, so that the total computation error meets the final target precision. Finite impulse response (FIR) digital filter is one of the fundamental components in digital signal processing and communication systems. It is also widely used in many portable applications with limited area and power budget.The proposed system presents a truncated multiplier design that can achieve faithful rounding results. Unlike previous related papers that manage to add some compensation circuits to reduce the truncation error, our new approach jointly considers the tree reduction, truncation, and rounding of the partial product bits during the design of fast parallel truncated multipliers so that the final truncated product satisfies the precision requirement**.**

II.TREE REDUCTION OF PARALLEL MULTIPLIERS

A tree based multiplier design usually consists of following major steps, i.e., PP (partial product)generation, PP deletion, PP reduction, truncation, rounding and final carry propagate addition. PP generation produces PP bits from the multiplicand and the multiplier. The goal of PP deletion and reduction is to delete some PP's and compress it, which is to be summed up by the final addition.

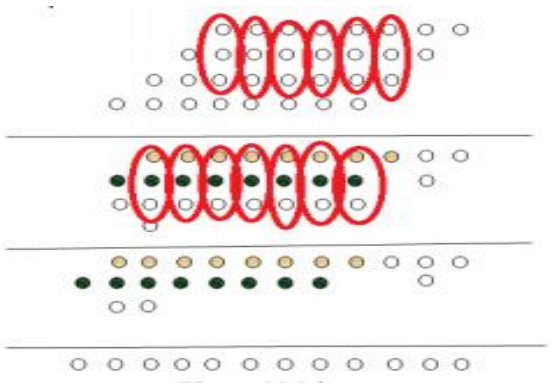

Figure Major steps

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Here we achieve around 33% area optimization and 20% Fmax enhancement with the same performance. The two most famous reduction methods are Wallace tree and Daddatree reductions. Wallace tree reduction manages to compress the PPs as early as possible, where as Dadda reduction only performs compression whenever necessary without increasing the number of carry-save addition (CSA) levels. Here we design a multiplier based on Wallace tree only.

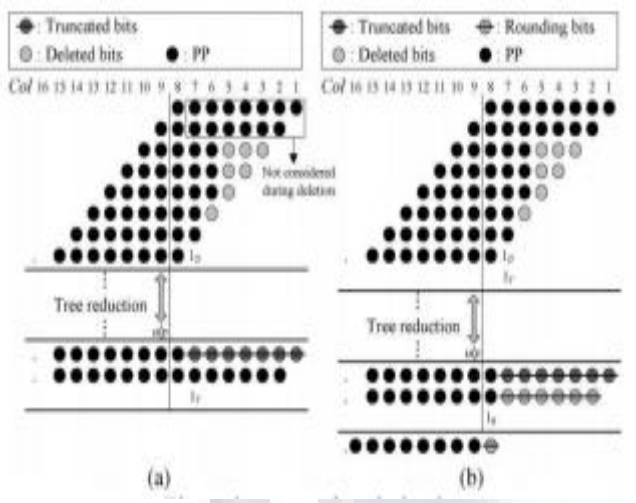

Figure proposed optimization

III. LITERATURE SURVEY

A faithfully rounded truncated multiplier design is presented where the maximum absolute error is guaranteed to be not more than 1 unit of least position. In there proposed method, they jointly considers the delete non require bits, reduce the level, truncation, round up result using correction logic and final addition of partial product bits in order to minimize the number of full adders and half adders during tree reduction. In this method efficiency of the proposed faithfully truncated multiplier with area saving rates of more than 30%. In addition, the truncated multiplier design also has smaller delay due to the smaller bit width in the final carry-propagate adder. The faithfully truncated multiplier has a total error of no more than 1 ulp and can be used in applications which need accurate result. By using this method we can be easily extended to signed or Booth multiplier design [1]. Low-cost finite impulse response (FIR) designs are presented using the concept of faithfully rounded truncated multipliers. They jointly consider the optimization of bit width and hardware resources without sacrificing the frequency response and output signal precision. Non uniform coefficient quantization with proper filter order is proposed to minimize total area cost. Multiple constant multiplications-accumulations in a direct FIR Structure is implemented using an improved version of truncated multipliers. Compare to other FIR design approaches show that the proposed designs achieve the best area, delay and power results [2].

IV. REDUCTION SCHEMES OF PARALLEL MULTIPLIERS

PP (partial product) generation produces partial product bits from the multiplicand and multiplier. PP reduction is used to compress the partial product bits to two. Finally the partial products bits are added by using carry propagate addition. Two famous reduction methods are available,

1. Dadda tree
2. Wallace tree

Dadda reduction performs the compression operation whenever it required. Wallace tree reduction always compresses the partial product bits. In this proposed work standard parallel multiplier is design & truncated multiplier design, introduces column-by-column reduction. The result is obtained from standard parallel multiplier and truncated multiplier gives close result. Truncated multiplier minimizes the half adders in each column because the full adder has high compression rate when compared to HA. A parallel tree multiplier design usually consists of three major steps, i.e PP generation, PP reduction, and final carry propagate addition. PP generation produces PP bits from the multiplicand and the multiplier. The goal of PP reduction is to compress the number of PPs to two, which is to be added for final addition. Wallace tree reduction manages to compress the PPs as early as possible, whereas Dadda reduction only performs compression whenever.

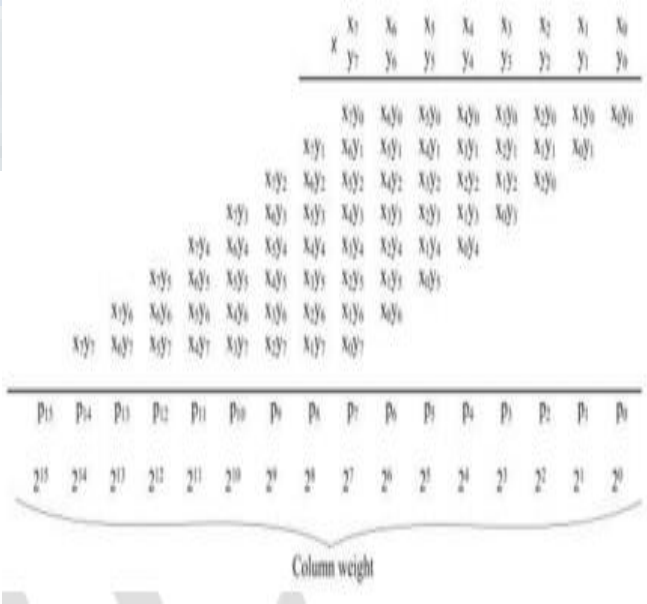

Fig. Standard parallel 8 x 8 bit multiplier

In this proposed work we first design standard parallel 8x8 multiplier which gives following result.

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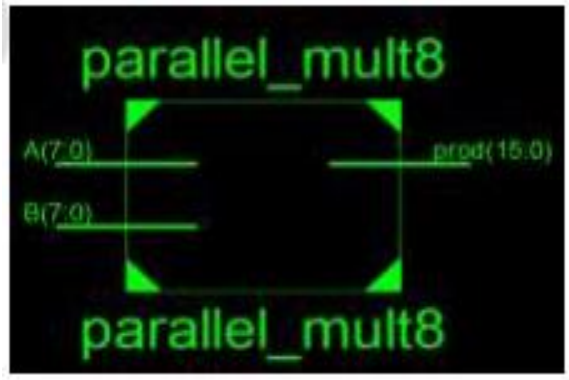
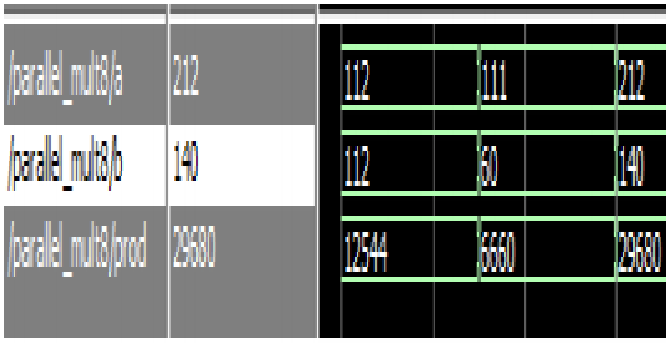


Fig. Block diagram of 8 x 8 parallel multiplier



This standard parallel 8x8 multiplier provides accurate result but requires large number of component to design by virtue of its area requirement is more. Also it requires more power and propagation delay. To reduce this requirement of area, power and delay we proposed truncated multiplier.

V. DELETION, REDUCTION AND TRUNCATION

In the first step, we perform the deletionthat removes all the unnecessary PP bits that do not need to be generated, as shown by the gray dots in Fig. 2 for an example of 8×8 unsigned fractional multiplication with eight product bits truncated. In this step, we delete as many PP bits as possible, for as long as deletion error EDis bounded by −1/2 ulp≤ ED≤ 0. After injection of a correction bias constant of 1/4 ulp, as shown by 1D in Fig.2 (a)

$$\frac{-1}{4}ulp < E_D \leq \frac{1}{4}ulp$$

The deletion error after the bias adjustment is note that the deletion of PP bits starts from column 3 by skipping the first two rows of PP bits because after applying reduction, the resultant two rows will be removed in the subsequent truncation and rounding processes to be described later. After the deletion of PP bits, we perform the per-column reduction of Scheme 2, as mentioned in Section II, and generate two rows of PP bits. After reduction, we perform the truncation that further removes the first row of n − 1 bits from column 1 to column n − 1, as shown by the crossed gray dots in Fig.2.This step of truncation introduces truncation error as

$$\frac{1}{2}ulp < E_T \leq 0$$

Again, after injecting another bias constant of 1/4 ulp, as shown by 1T in Fig.2, the adjusted truncation error is bounded by

$$\frac{-1}{4}ulp < E_T \leq \frac{1}{4}ulp$$

VI. ROUNDING AND FINAL ADDITION

After deletion, reduction, and truncation, the PP bits are added using a CPA to generate the final product of P bits, as shown in Fig. 2(b). Note that the bits in column 2 to column n − 1 [as highlighted by crossed spotted dots in Fig. 2(b)] can be safely removed before CPA because these bits are the only bits left in the columns after the deletion and truncation processes, and thus, they do not affect the carry bit to column n + 1 (the column with a weighting of 1 ulp) during the rounding process. Before the final CPA, we add a bias constant of 1/2 ulp, which is shown as 1R in Fig. 2, in order to achieve the round-to nearest rounding with the rounding error.

$$\frac{-1}{2}ulp < E_R \leq \frac{1}{2}ulp$$

The bit at column n after the final CPA is also removed during the rounding process. Thus, the total error for the design of the faithfully rounded truncated multiplier is bounded by

$$-\text{ulp} < E = (E_D + E_T + E_R) \leq \text{ulp}$$

Note that the proposed truncated multiplier design achieves faithful rounding because the total error is no more than 1 ulp. Furthermore, the three bias constants, i.e., 1D, 1T , and 1R, can be collected into a single constant bit to be added at column n + 1, without increasing the overall height of the PP matrix.

VII.PROPOSED ALGORITHM

In proposed architecture we multiply 8 x 8 bits, and the bits are reduced in step by step manner. Deletion is the first operation performed in Stage 1 to remove the PP bits, as long as the magnitude of the total deletion error is no more than 2-P-1 . Then numbers of stages are reduce the final bit width without increasing the error. Fig. shows proposed truncated multiplier. This reduces the area and power consumption of the multiplier [3]. For this we used Half Carry (HC), Full Carry (FC), Half Adder (HA), Full Adder (FA) logic to improve the result. Requirement of component for this truncated multiplier is less as compared to standard parallel multiplier; however it reduces the area required as

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well as delay and power. Following result is obtained for proposed 8 x 8 bit truncated multiplier which is approximately same as that of standard parallel multiplier with precision improvement.

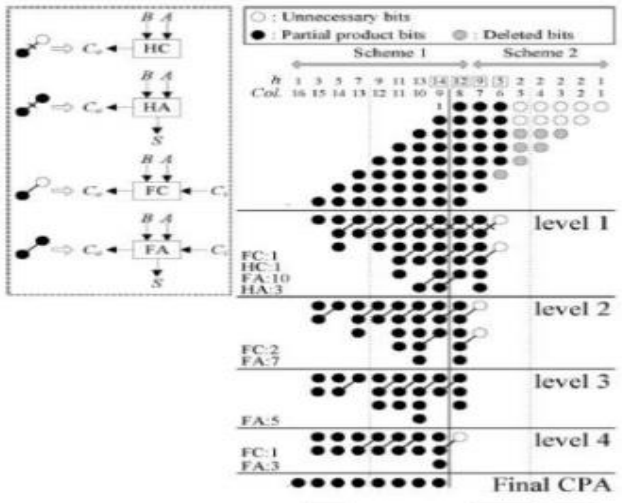


Fig. Proposed 8 x 8 bit truncated multiplier

The truncated multiplier for general M × N unsigned multiplication with a full product of M+N bits truncated to P bits. In other words, there are T = M + N – P bits truncated . First, perform deletion in stage 1 to remove the PP bits, as long as the magnitude of the total deletion error is not more. Bits[Col] represents the number of PP bits of column Col. Note that the first two rows of PP bits from column 1 to column T 1 are kept unchanged during the deletion process. Note that at column T + 1, we add a constant of which is the sum of the three constants (1D, 1T, and 1R) in the aforementioned deletion, truncation, and rounding. In stage 2, for column Col, determine whether an HA is required or not (HA[Col] = true or false) and find the number of carry bits to the next column. Furthermore, according to this experiments, it is observed that HAs should be used as early as possible in order to reduce the critical path delay because HAs have a smaller pin-to-pin delay compared with FAs. In stage 3, tree reduction is performed along with truncation and rounding. For the final two rows of PP bits from column 1 to column T − 1, there no need to generate these PP bits because they will be removed during the subsequent truncation and rounding processes. For example, in figure the two white dots at level 1 and the two white dots at level 2 are not generated during the compression with FAs or HAs. Thus, in this introduce two simplified versions of the FA and HA cells, i.e., full and half adders without the sum output bits. For column T, only need to generate the carry bit (to column T + 1) for the last FA compression because the sum output bit will be discarded during the rounding process. For example, the FA compression does not need to generate the white dot (the sum output bit) at level 4 of figure. Note that for column T + 1 to M + N, although it is adopted to determine whether an HA is needed or not, we actually do not compress the column height to one because this compression will cause ripple carry. Indeed, at the last level of the reduction process, some column, for example column i, has a height of three, and the remaining columns beyond this specific column, i.e., columns i +1, i + 2….., have a column height of two, as shown in level 4 of figure. Afterward, a final CPA performs the final summation. In the example in figure, the bit width of the final CPA is 7.

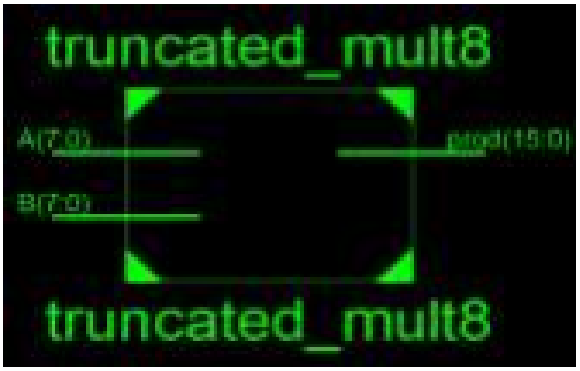
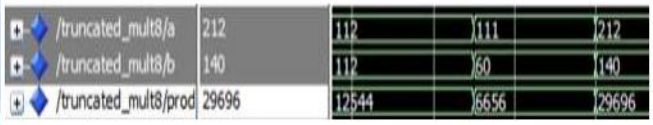


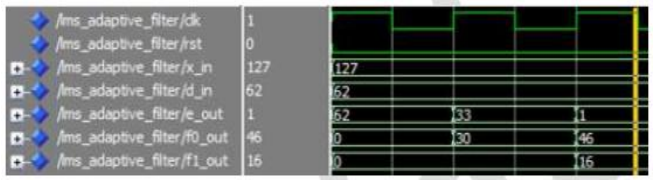
Fig. Block diagram of 8 x 8 bit truncated multiplier



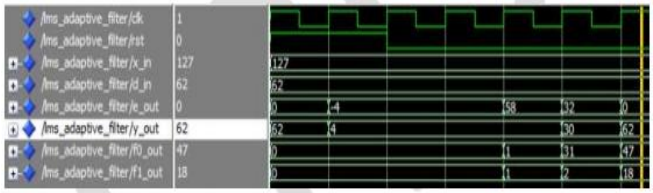
This truncated multiplier is proposed multiplier for DSP applications. For this truncated multiplier there are different logic is applied such as deletion, reduction, truncation, rounding and final addition. It is providing multiplication of 8 × 8 bit which gives approximate result

For FIR filter with standard 8 × 8 bit parallel multiplier

This simulation is for 2-Tap Adaptive FIR filter with standard parallel multiplier. From this it is clear that error continuously tending towards zero.



For FIR filter with 8 × 8 bit truncated multiplier



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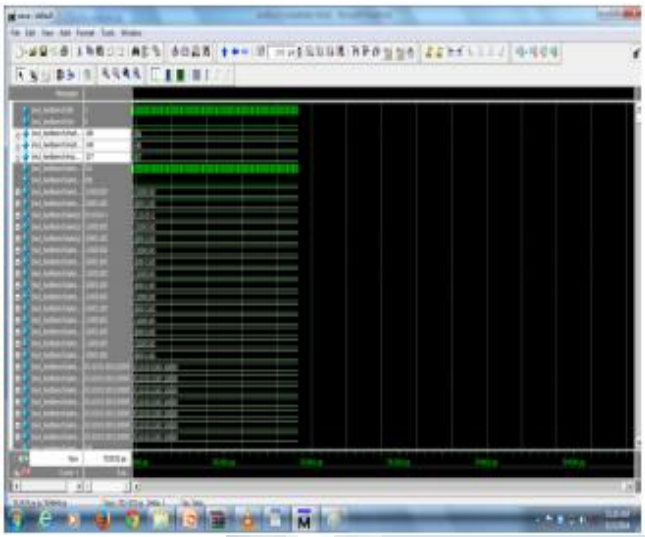
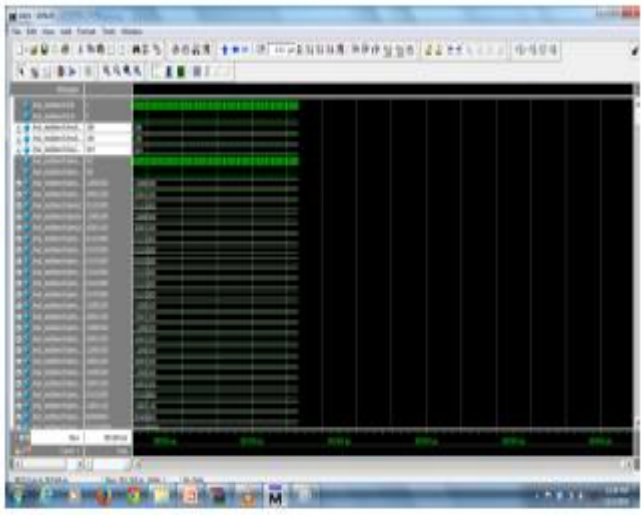
VIII.EXPERIMENTAL RESULTS

Model Sim Output: Direct Truncation



Quartrus ii 9.0 web edition output

MODELSIM OUTPUT TREE BASED TRUNCATION



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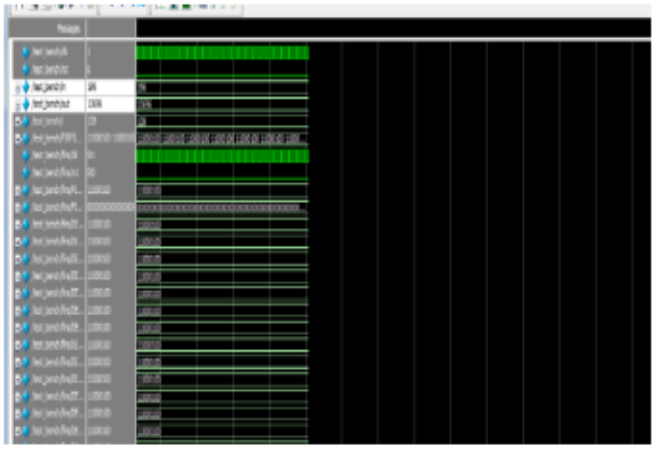
FIR FILTER OUTPUT DIRECT TRUNCATION



Area utilization

IX. CONCLUSION AND FUTURE WORK

It is concluded that tree based truncation in FIR filter gives better hardware complexity and power optimization with reduced delay. This method avoids the use of a large area in terms of logic elements.Modelsim based simulation results of an implementation of truncated multiplier in FIR filter showed the feasibility of this approach. QUARTUS II based hardware synthesis report of truncated multiplier in FIR filter consumes estimated power of 39.54 mW and occupies an area of 210 nm which is less when compared to a direct truncation multiplier.

Field programmable gate arrays were actually invented only for prototyping the digital design which is later to be used in IC's. But in recent days FPGA's are started to use as a product in many fields. So Field programmable gate arrays are ideally suited for the implementation of truncated multiplier in FIR filter which is used for signal processing applications. However, there are several issues that need to be solved. When performing software simulation of truncated multiplier, calculations are carried out with decimal point. But in FPGA only integer arithmetic points are used which is unjustified, and measures tobe takento account for this. Many techniques have been used to efficiently use floating point (IEEE 754 format) values into for digital implementation. Then only we can implement truncated multiplier in VLSI.

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