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AN EFFICIENT REVERSE CONVERTER DESIGN VIA PARALLEL PREFIX ADDER

[#1]BEERAM SANDHYARANI, M.Tech Student,
[#2]R.NARAIAH, Associate Professor,
Department Of ECE
VAAGESHWARI COLLEGE OF ENGINEERING, KARIMNAGAR, TELANGANA, INDIA.

ABSTRACT: In this paper, the implementation of residue number system reverse converters based on hybrid parallel prefix adders is analyzed. The parallel prefix adder provides high speed and reduced delay arithmetic operations but it is not widely used since it suffers from high power consumption. Hence, a hybrid parallel prefix adder component is presented to perform fast modulo addition in Residue Number System reverse conversion. The proposed components are not only results in fast arithmetic operation and it also highly reduced the hardware complexity since it requires fewer amount of logic elements. In this work, the proposed components are implemented in different moduli sets reverse converter designs and the performances are compared for different values of n.

Keywords: *Digital arithmetic, parallel-prefix adder, residue number system (RNS), reverse converter.*

I.INTRODUCTION

The Residue Number System plays a significant role in the battery based and portable devices because of its low power features and its competitive delay. The Residue number system reverse converter is designed with parallel prefix addition by using new components methodology for higher speed operation. The RNS consists of two main components forward and the reverse converter that are integrated with the existing digital system. The forward converter performs the operation of converting the binary number to the modulo number whereas the reverse converter performs the operation of reverse converting the modulo number to the binary number which is the hard and time consuming process compared with the forward converter. The fundamental RNS concepts such as 1)RNS definition with properties and their applications,2)consideration of modulo set selection,3)design of forward converter,4)modulo arithmetic units,5)design of reverse converter are discussed. The voltage over scaling (VOS) technique is applied to the residue number system to achieve high energy efficiency. The VOS technique introduces soft errors which degrades the performance of the system. To overcome these soft errors a new technique is implemented called joint RNS-RPR (JRR) which is the combination of RNS and the reduced precision redundancy. This method provides the advantage of satisfying the basic properties of RNS includes shorter critical path, reduced complexity and low power. New architectures are presented for the moduli set (2n-1,2n, 2n+1) for the conversion from the residue to the binary equivalents. Here the speed and the cost are major concern. Distributed arithmetic principles are used to perform the inner product computation. The input data which are in the residue domain which are encoded using the Thermometer code format and the outputs are encoded using the one hot code format. Compared to the conventional method which used Binary code format, the proposed system which achieves higher operating speed. The residue number system which provides carry free addition and fully arithmetic operation, for several applications such as digital signal processing and cryptography. In this brief, we present a comprehensive method which uses the parallel prefix adder in selected position, thereby using the shift operation on one bit left to design a multiplier on the same design module to achieve a fast reverse converter design. The usage on parallel prefix structure in the design leads to higher speed in operation meanwhile it increases the area and power consumption. In order to compensate the tradeoff between the speed, area and power consumption, a novel specific hybrid parallel prefix based adder components are used to design the reverse converter. These hybrid design which provides the significant reduction in the power delay product (PDP) metric and leads to considerable improvements in the area time² product (AT^2) in comparison with the traditional converters without using parallel prefix adders.

more complex and non-modular structure. So the process of reverse converting is tough and time consuming process. Therefore more care should be given to its design in order to avert slow operation and without compromising the benefits of RNS. In reverse converter design the value of moduli of the moduli set must be substituted in conversion algorithm formulas obtained from Chinese remainder theorem (CRT) [5], mixed radix conversion (MRC) [4], and new Chinese remainder theorem. The final equation from conversion theorem should be simplified by using some properties and the final binary representation is recognized using the adder. Usually the design of the reverse converters is done using the parallel prefix adders for higher speed operation. But it

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suffers from higher power consumption. The parallel prefix adders are more flexible and used to increase the speed in binary additions

II.LITERATURE REVIEW

The reverse converter design is non-modular process and it is more complex. To design a reverse converter there are some design procedures. The arithmetic units are the prime concern in the residue based digital systems. To make efficient design of reverse converter, we consider mainly two factors to improve the performance of the converters: 1)Explore new algorithms and novel arithmetic formulations to achieve simplified conversion formulas. 2) Introduce new moduli sets, which can lead to more simple formulations. The modulo adders are the conventional resources that are used in reverse converters. The modulo ripple carry adder will have simple structure yet touches from longer propagation delay whenever number of bits are growing for the inputs. To perform conversion earlier we introduced few converters, converter with carry save adder lags in speed. Then the carry propagate adder based converter is presented which is less complex. In this adder when number of residues is increasing, the carry has to propagate from one stage to another stage to compute the sum which in turn induces the delay. To improve the speed, high speed parallel prefix adder converters are introduced. These will produce the carry at the preceding stage such that it will directly compute the sum from the carry results which are obtained at the previous stage. But this parallel prefix adder is having huge area and power consumption which degrades the performance of the converter. So we designed a converter such that optimizes needs minimum area and good amount of speed. We have introduced new hybrid parallel prefix converters which are efficient in area with compared to the regular prefix adders and speed efficient with compared to the Carry propagate adders based converter. This hybrid parallel prefix adder structure introduced provides a better tradeoff between the delay and power consumption.

III.PARALLEL PREFIX STRUCTURE

The Residue number system mainly composed of three main parts such as, forward converter, modulo arithmetic units and reverse converter. On comparing with the other parts the reverse converter design is a complex and no modular structure. So more attention is needed in designing the reverse converter thereby preventing the slow operation and compromises the benefits of the RNS.The parallel prefix structure helps to achieve the faster operation in the reverse converter design but causes increased power consumption. In the existing system the novel specific hybrid parallel prefix adder based components are used to replace the existing components there by reducing the power consumption and getting faster operation.

A. Parallel Prefix Block

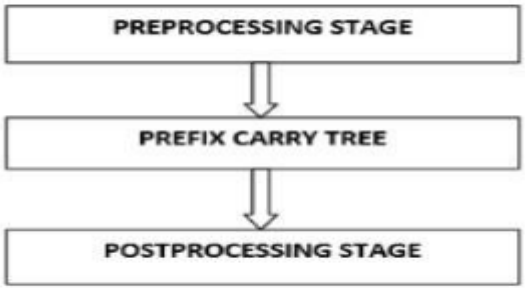

Fig.1 Basic Parallel prefix structure

The Parallel prefix structure consists of three main blocks, they are preprocessing block, prefix carry tree and post processing block. The parallel prefix adder operation begins with preprocessing stage by generating the Generate (Gi) and Propagate (Pi) equation[1]&[3].The prefix carry tree get proceeded with the previous block signal to yield all carry bit signal and these stage contains three logic complex cells such as Black cell, Gray cell and Buffer cell. Black cell compute both the propagate (P(i,j)) and generate (G(i,j)) by using the equation[3]&[4].The Gray cell executes only the generate(G(i,j)).The carry bits generated in the second stage get passed to the post processing block thereby generating the sum using the equation[5].The block diagram is shown in the Fig1.

Gm:n=An AND Bn (1)
G0 =Cin (2)
Pm:n=An XOR Bn (3)
P0=0 (4)
Gm:n=Gn:k OR Pn:k AND Gk-1:n (5)
Pm:n=Pn:k AND Pk-1:j (6)
Sn =Pn XOR Cin (7)

The Brent Kung adder prefix structure is employed to achieve the higher speed with reduced power consumption. On comparing with the other parallel prefix adder structure the BK adder is chosen mainly for minimum fan-out and should be higher speed in operation than others.Fig.2shows the example BK adder prefix structure which uses the three basic cells in the prefix structure. These structure is elaborated for the proposed design having the modulo addition of (4n+1) for n=5.

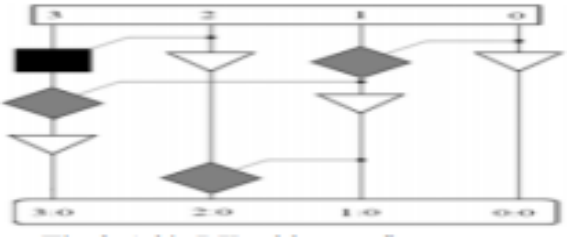

Fig.2:4-bit BK adders prefix structure

B.HRPX Structure :(Hybrid Regular Parallel prefix XOR/OR adder component)

Fig.3 shows HRPX Structure. The regular parallel prefix adder is used to do the first part of addition and the

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simplified RCA logic is used to do the second part where the corresponding bits of the operand are fully variable. Full adder can be designed with XOR/OR gates because of the constant operand. In these reverse converters design the carry chain is not needed and can be ignored. For most modulo sets (2^n-1) addition is a necessary operation. The End around Carry (EAC) for (2^n-1) addition is represented with two zero, but for the reverse converter design one zero representation is required. To correct these zero representation problem, a detector circuit was employed in the design but it incorporates additional delay. So, the Binary to excess one converter (BEC) is used to solve the double zero representation issue.

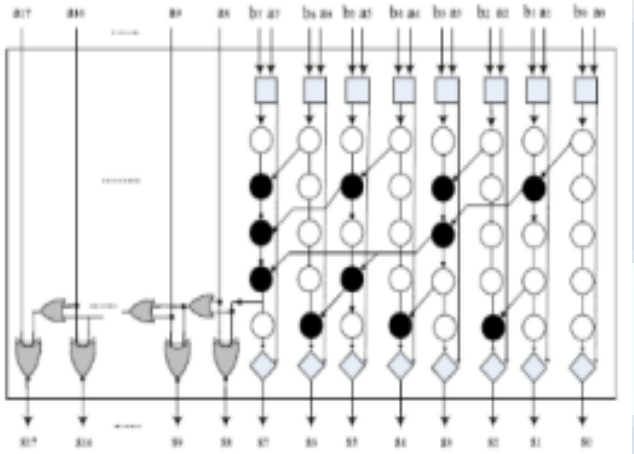

Fig.3 HRPX Structure using BK prefix network

IV.NEW PARALLEL-PREFIX-BASED COMPONENTS

The HMPE Structure consists of two parts: Regular prefix adder and the Modified Excess One unit. The first two operands are added using the parallel prefix adder and the result is conditionally incremented based on the control signal generated by the prefix structure to assure the single zero representation.The below figure shows HMPE Structure.

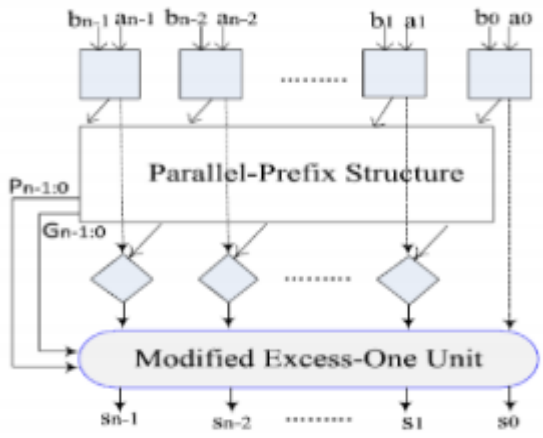

Fig.4: HMPE Structure

Modified Excess One unit Description

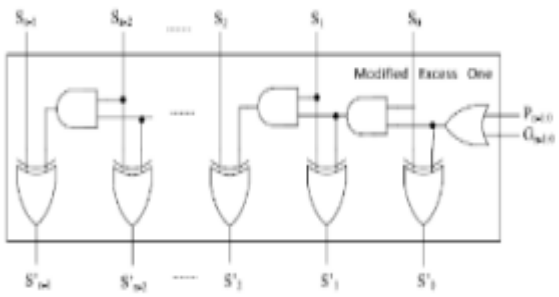

Fig.5: Modified Excess one unit

Fig.5 shows the Modified Excess One unit circuit diagram. The result generated by the prefix structure is conditionally incremented by this unit based on the control signal generated by the parallel prefix adder. The reverse converter design is implemented for (4n+1) modulo addition (n=5) designing the adder and also the multiplier by using the same adder design without using any parallel prefix multiplier structure for designing multiplier. In this design, the adder design is implemented by using the Kogge Stone adder parallel prefix structure. Here the first two operands are added by using the prefix adder preprocessing stage thereby generating the propagate and generate equation. The first stage processed signal get passed to the next stage called the prefix carry tree, this stage again computes the generate and propagate equation by using the previous output and all the logic cells employed in the Kogge Stone adder network. These processed signals are passed to the post processing block.

V.REVERSE CONVERTER DESIGN METHODOLOGY

In this section, the methodology of reverse converter design is described. In the following, a method employing distinct components in the architecture of the reverse converter will be presented. Several reverse converters for different moduli sets have been introduced, which can be classified into three classes. The first class consists of converters with a tree of CSAs with EAC followed by a two-operand modulo $2k - 1$ CPA. A second class includes more complex reverse converters, which have several CSAs and CPAs with EACs followed by a final regular subtractor with two operands of different size. The implementation of this subtractor using regular binary-adder results in one operand with some constant bits. The third class covers the reverse converters that have been designed for moduli sets with moduli other than the popular $2n$ and $2n \pm 1$. In the following, we describe a methodology for designing reverse converters in the first and second classes. The suggested method for applying the HMPE and HRPX in the reverse converter is shown in Fig.6.

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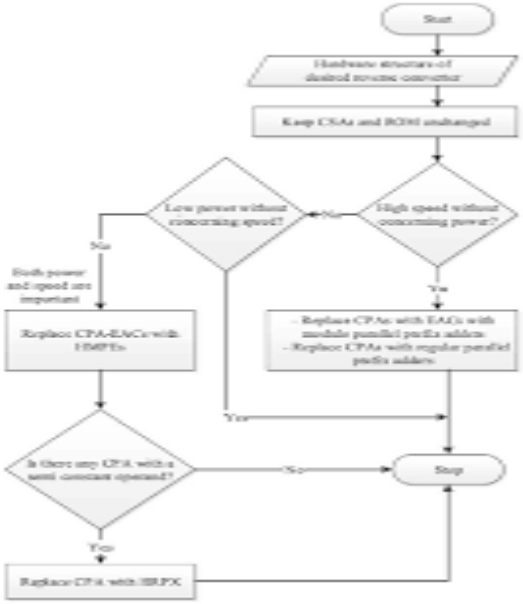

Fig.6: Reverse converter design methodology

If it is just important to achieve the least power consumption and hardware cost without considering speed, no prefix adder is needed. On the other hand, if high speed is the designer goal, the CPAs with EAC and the regular CPAs should be replaced by traditional parallel prefix modulo 2n – 1 adders and regular parallel-prefix adders, respectively. However, for the VLSI designers, a suitable tradeoff between speed, power, and area is often more important. In this case, first, CPAs with the EAC can be replaced by the HMPEs. Then, if the converter contains a regular CPA where one of its operands has a string of constant bits with the value of one, it can be replaced with the HRPX.

VI.BRENT-KUNG ADDER

The Brent-Kung adder is a parallel prefix adder[13]. Parallel prefix adders are distinctive type of adders that are based on the use of generate and propagate signals. Simpler Brent-Kung adders was been proposed to solve the disadvantages of Kogge-Stone. The parallel Prefix based Brent Kung Adder (BK) components provides a better tradeoff between power and area. However the large number of levels in BK adder reduces the operational speed. BK adder is known for its high logic depth with minimum area characteristics.

VI. KOGGE STONE ADDER

Kogge-Stone adder is a parallel prefix form carry look ahead adder [11]. A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes. The time required to generate carry signals in this prefix adder is o (log n). It is a fastest adder design and common design for high performance adders in industry . A significant delay reduction and area x time2 improvements are the advantage of Kogge–Stone (KS). But the cost of high power consumption is the main reason for preventing the use of parallel prefix Kogge Stone adder. In the system, we use a proposed prefix adder, in this adder we take the first stage of BK and rest of the stages remain as KS adder. In this adder it consists of three stages they are pre-processing stages, carry generation network and post-processing stage.

In the pre-processing stage it will pre-computes the carry generate and carry propagate signals.

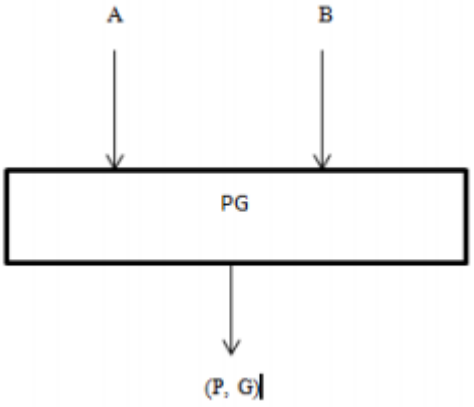

Fig.5. propagate and generate block

It takes inputs (a, b) and compute generate and propagate bits using below equations. It uses an XOR and AND gates to generate the output.

G= A.B

P=A XOR B

VIII.EXPERIMENTAL RESULTS

8.1Simulation Results:

The simulation process has been carried out for different levels of abstraction. The code has been written in Verilog hardware description language. The top module has been synthesized and simulated in Xilinx ISE Design Suite 12.3 and the corresponding delay calculations have been noted. By using Kogge Stone Adder the delay and area was reduced.

Simulation results are shown in fig 7 and 8. RTL Schematic diagrams are shown in fig 9 and 10.The design was implemented in Spartan-3E kit.

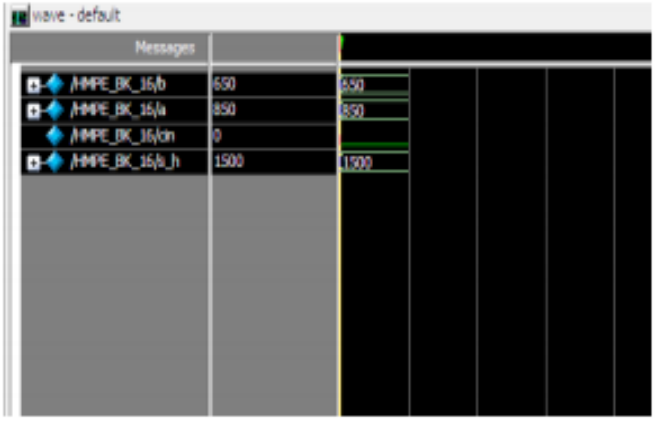

Fig.7: Simulation result of HMPE-BK Adder Parallel Prefix Structure

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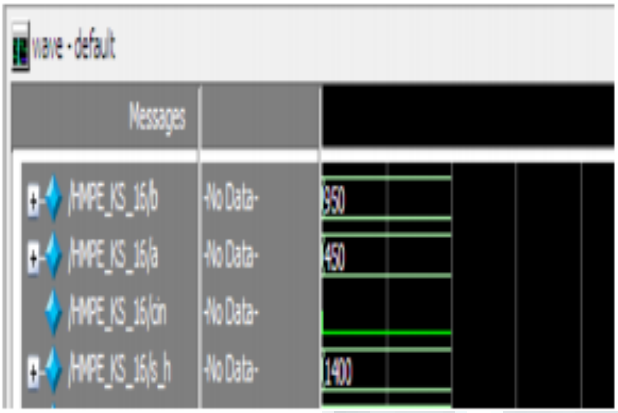

Fig.8: Simulation Result of HMPE-KS Adder Parallel Prefix Structure

8.2: RTL (Register Transfer Level) schematic diagrams:

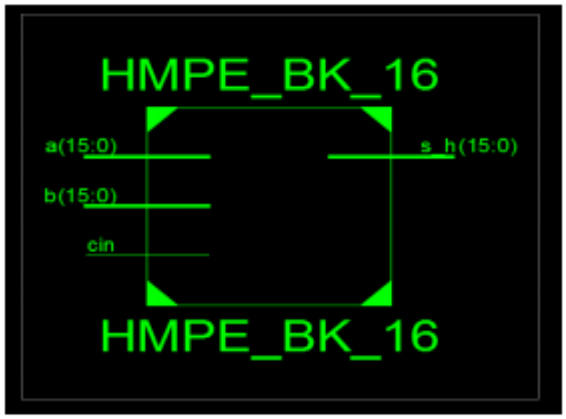

Fig.9: RTL Schematic of HMPE- BK Adder Parallel Prefix Structure

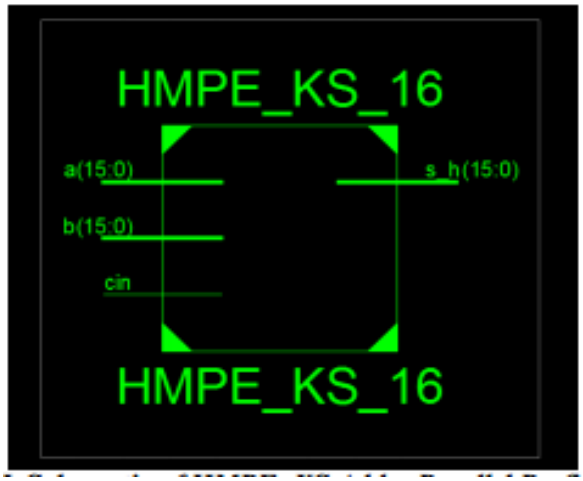

Fig.10: RTL Schematic of HMPE- KS Adder Parallel Prefix Structure

5.3: Synthesize Result:

Table shows the synthesize result for using Xilinx project navigator for device xc3s400-4pq208.

Table Synthesize result

	HMPE-BK	HMPE-KS
DELAY(ns)	31.83	29.02
POWER(mW)	56	56

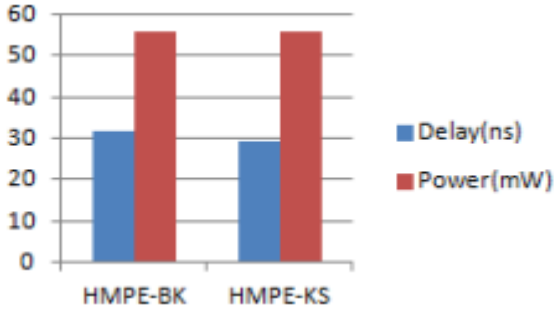

Fig.11: performance and power trade-off of different system

IX.CONCLUSION

This proposed work presents hybrid parallel-prefix-based adder components that give better tradeoff in area and delay are thus exhibited to design reverse converters. A methodology is described to design reverse converters depending on various types of prefix adders. These components are particularly designed for reverse converters. Implementation results gives that the reverse converters depending on the suggested work significantly decreases the area and delay when contrasted and the original converters, which don't utilize any parallel-prefix adders. Future work includes the extension of the bit size and to construct an efficient reverse converter.

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