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AN EFFICIENT DESIGN AND IMPLEMNTATION OF HIGH-PERFORMANCE NOISE-TOLERANT XOR-XNOR CIRCUITS

[#1]K.PRIYANKA, M.Tech student,
[#2]R.NARAIAH, Associate Professor,
Dept of ECE,
VAAGESHWARI COLLEGE OF ENGINEERING, KARIMNAGAR, TELANGANA,INDIA.

ABSTRACT: A three-input XOR/XNOR as one of the most complex and all-purpose three-input basic gates in arithmetic circuits. In this brief, we propose three efficient three-input XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybrid-CMOS logic style. This structure is generated systematically by employing binary decision diagram. After that, concerning high flexibility in design targets, SCDM aims to specific ones in the remaining three steps, which are wise selections of basic cells and amend mechanisms, as well as transistor sizing. In the end, the resultant three-input XOR/XNORs enjoy full-swing and fairly balanced outputs. I design a XOR/XNOR circuits using QLQT, in order to improve the reliability of the circuit. The dynamic voltage scaling is used to reduce power.My proposed method will be implemented in TINA and Xilinx Spartan 3 processor.

Keywords: *systematic cell design methodology, Quadded logic with quadded transistor.*

I. INTRODUCTION

Chip designs are developed with several different methodologies. High-end ICs are often developed with a full custom methodology because they require a very high level of performance. This performance can only be achieved by extreme customization of the design including custom macro cells, circuits using dynamic logic, transistor-level tools and handcrafted layout. This methodology gives designers more flexibility to tune the performance of a design commensurate with power requirements. However, a full-custom design methodology is very costly in terms of resources and design talent. It requires a large team of engineers and too much time to complete these designs. On the other hand, many semiconductor products are developed with a semi-custom design methodology based on standard cell libraries, synthesis and place-and-route tools. This methodology is very attractive, as time-to-market pressures demand increasingly shorter completion times to meet product goals. Using such methodologies, engineers can focus on describing the design and the flow to ensure that the design is implemented in silicon within an expeditious timeframe. But the performance of such designs is limited. Standard cell libraries using standard CMOS logic are provided by several companies for all manufacturing technologies and are widely available. The same cannot be said for novel circuit realization techniques. Until their commercial viability is proven few companies find it a worthwhile investment to provide a standard complete cell library for a new circuit design technique. Some academic and research institutions have tried designing small-scale libraries (with perhaps 50 cells) but such efforts seldom result in a library that is comparable to those provided for standard CMOS design. The advent of relatively inexpensive LSI technology and the increasing demand for fault-free operation of digital systems for long periods of time have rekindled the interest in fault tolerant computer design. In order to predict the performance of a particular design or compare two or more designs, an accurate reliability model is needed. A various switch designs for the hybrid redundancy scheme. It will be shown that the switch reliability is an important factor in determining the overall system reliability. The current effort is directed towards obtaining a suitable model for the switch designs. A model will be presented and it will be used to compare the various designs. First we will present the redundancy schemes to be studied. Advances in fabrication technology have made integrated circuits more prone to manufacturing variations, aging, and/or soft errors. This is of significant concern in many safety-critical applications, such as medical devices and aerospace applications. Fault-tolerance has become an integral part of digital circuit and system design.

In this paper, we present a formal design method for balanced 3-input XOR–XNOR circuits in the hybrid-CMOS logic style. In our approach, we start with selecting a basic cell including 3-input and two outputs. Next and if necessary we apply various correction mechanisms and optimization methods to obtain balanced 3-input XOR–XNOR circuits. Accordingly and by using four basic cells, we come up with six balanced 3-input XOR–XNOR circuits. In any type of logic design, the non full-swing outputs play a decisive role in cell drivability. Full swing outputs impact multi-stage structured arithmetic circuit performance [12][13]. Therefore, designers consider achieving full swing output operations as an important factor in the basic block

design of arithmetic circuits. In addition, all of the proposed circuits whose critical path contains only two transistors have low average power consumption and delay. The proposed circuits features balanced outputs, making it easy for large tree structured arithmetic circuits to maximize area efficiency without unduly degrading the VLSI power and delay. The rest of this paper is organized as follows. Section 2 begins with the introduction of the design methodology, and the structure of the elementary basic cell. We use this basic cell and introduce two different alternative basic cells based on pass transistor and transmission gate. In addition, we state optimization and correction mechanisms shortly. In Section 3, we introduce six novel balanced 3-input XOR/XNOR circuits using basic cells in conjunction with the mechanisms. In Section 4, we report simulation results. We analyze the method in Section 5. Finally, we offer concluding remarks in Section 6.

II.FAULT DETECTING METHODS

In reliability engineering, dual modular redundancy (DMR) is when components of a system are duplicated, providing redundancy in case one should fail. It is particularly applied to systems where the duplicated components work in parallel, particularly in fault-tolerant computer systems. A typical example is a complex computer system which has duplicated nodes, so that should one node fail, another is ready to carry on its work. DMR provides robustness to the failure of one component, and error detection in case instruments or computers that should give the same result give different results, but does not provide error correction, as which component is correct and which is malfunctioning cannot be automatically determined. There is an old adage to this effect, stating: "Never go to sea with two chronometers; take one or three. A lockstep fault-tolerant machine uses replicated elements operating in parallel. At any time, all the replications of each element should be in the same state. The same inputs are provided to each replication, and the same outputs are expected. The outputs of the replications are compared using a voting circuit. A machine with two replications of each element is termed dual modular redundant (DMR). The voting circuit can then only detect a mismatch and recovery relies on other methods. A machine with three replications of each element is termed triple modular redundant (TMR). The voting circuit can determine which replication is in error when a two-to-one vote is observed. In this case, the voting circuit can output the correct result, and discard the erroneous version. After this, the internal state of the erroneous replication is assumed to be different from that of the other two, and the voting circuit can switch to a DMR mode. This model can be applied to any larger number of replications. In computing, triple modular redundancy, sometimes called triple-mode redundancy, (TMR) is a fault-tolerantform of N-modular redundancy, in which three systems perform a process and that result is processed by a majority-voting system to produce a single output. If any one of the three systems fails, the other two systems can correct and mask the fault. The TMR concept can be applied to many forms of redundancy, such as software redundancy in the form of Nversion programming, and is commonly found in fault-tolerant computer systems. Some ECC memory uses triple modular redundancy hardware (rather than the more common Hamming code), because triple modular redundancy hardware is faster than Hamming error correction software.[2] Space satellite systems often use TMR, although satellite RAM usually uses Hamming error correction.

A.REDUNDANCY SCHEMES

Hardware redundancy may be used in a variety of manners to achieve fault tolerance. Among the best known techniques are the replication schemes, such as triple modular redundancy (TMR) and N-modular redundancy (NMR). TMR, first proposed by Von Neumann, divides a non redundant circuit into modules and replicates each module thrice. The most widely used fault-tolerant methods used to mitigate logic errors in FPGA designs rely on hardware redundancy: 1) duplication with comparison (DWC) for detecting faults and 2) triple modular redundancy (TMR) with majority voter for masking faults. In DWC, the original block to be protected is replicated twice and the results produced by the original and the outputs of replicated blocks are compared to detect faults. The lockstep scheme is the implementation of DWC at the processor level, supported by some Xilinx FPGAs. Two identical processors _P1 and _P2 receive the same inputs, simultaneously execute the same instructions, and their results are compared step-by-step at each clock cycle. _P2 generates the reference results to be compared against those of _P1 that provides the system output. Basically, DWC is able to detect but not to correct errors, because it cannot point out the faulty processor. However, it could be capable to tolerate temporary faults, provided that it is supported by some reexecution procedure. In case of FPGA implementation, the system needs also to be reconfigured to recover correct functionalities. In TMR, the original block is replicated thrice, all three blocks receive the same inputs, and a majority 2-out-of-3 voter is used to determine the correct result. It is also possible to detect inconsistencies in the outputs of the three blocks to identify the faulty one. TMR allows to mask directly both temporary and permanent faults of a single block.DWC and TMR are conceptually relatively simple and easy to implement in FPGA. Unfortunately, they are also very costly, because they involve, respectively, over 100 and 200 percent hardware overhead. Therefore, they must be used skillfully to guarantee required reliability level at the minimum cost.

One of the wellknown and widely used fault-tolerant techniques in safetycritical applications is triple modular redundancy (TMR). A traditional TMR system consisting of three redundant modules and a voter at the modules outputs has some shortcomings that should be addressed in order to be employed in safety-critical applications. A major shortcoming of the traditional TMR is its inability to cope with TMR failures. TMR failure refers to a failure in a TMR system caused by multiple faulty modules or a faulty voter. Although the probability that two particles hitting two replica flip-flops in a TMR system is very low, the probability that two energetic particles hitting two modules of a TMR system is not very rare when the system is running in a harsh environment for long periods. In case of independent fault arrivals in two different modules, if neither of the faults is overwritten, it may result in a TMR failure. For long-term applications, the absence of appropriate recovery mechanisms significantly increases the probability of TMR failure occurrence. To address this issue, TMR should be equipped with a transient error recovery technique. Most of the previous TMR-based error recovery techniques proposed so far exploit retry mechanisms. These techniques, however, are not suitable for tight deadline applications, as the re-computation may result in a task completion after its deadline.A fault in a system is some deviation from the expected behaviour of the system: a malfunction.

III. SYSTEMATIC CELL DESIGN METODOLOGY

To optimize system area furtherly we use systematic cell Design Methodology(SDM) to design xnor gate in our encoder. we propose three efficient three-input XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybridCMOS logic style. SCDM, which is an extension of CDM, plays the essential role in designing efficient circuits. At first, it is deliberately given priority to general design goals in a base structure of circuits. This structure is generated systematically by employing binary decision diagram. After that, concerning International Journal of Engineering Science and Computing, May 2016 5098 http://ijesc.org/ high flexibility in design targets, SCDM aims to specific ones in the remaining three steps, which are wise selections of basic cells and amend mechanisms, as well as transistor sizing. In order to generate the EBC of three-input XOR/XNOR circuits, four steps are taken. The process has been shown in Fig. (1-4) Initially, three-input XOR and its complement is represented by one binary decision tree (BDT) in order to share common sub circuits. The BDT is achieved by some cascaded 2 ×1 MUX blocks, which are denoted by simplified symbol controlled with input variables at each correspondent level. This construction simply implements the minterms of the three-input XOR/XNOR function. The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. Afterward, as the inputs into the first level are 0's and 1's of the function's truth table, the 0 and 1 can be replaced by the Y and Y', respectively. Finally, the simplified symbol can be divided into two distinct symbols: 1) the plus sign with the x input control and 2) the minus sign with the x' input control. The result of applying steps 3 and 4 is shown in Fig. 3. The EBC, which is extracted from the above procedure, has been presented. This cell has eight elements, deciding two outputs. We refer to the pins of the central section (IN1–IN4 and G1– G4) as A or C, or their complements. We also assume that pins of the external section G5–G8 can also be B or its complement.

A. WISELY SELECTION OF MECHANISMS AND CELLS BASED ON DESIGN TARGET

By replacing the elements with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a huge circuit library is achieved as each circuit can be appropriate for specific applications. The selection is meditated to determine dominant mechanisms and cells, in terms of PDP, power, and delay when the optimization goal is PDP. The results are used to produce circuits for high-performance portable electronic applications. Mechanisms include optimization mechanisms to resolve non full swing [inverter (I) and feedback (F)], correction mechanisms to resolve high impedance [pull up down network (P) and feedback (F)], or the combinations of them [bootstrappull (BP) up-down, feedback pull (FP) up-down, bootstrapfeedback (BF), inverter feedback (IF), and inverter-pull (IP) up-down]. The cells are divided into three categories:

1) Cells with both nMOS and pMOS in EBC structure (C1);
2) Only nMOS (C2);
3) Only pMOS (C3).

To reduce complexity, we have also considered the central part of EBC and to achieve real results, the circuits have been simulated in the chain test bench. The circuits have been named with the abbreviation of the mechanism (or cell) being utilized, while the other circumstances, cells, or mechanisms are assumed to be fixed. Using transmission gates in EBC, which is called TG, the complete circuit is achieved as there is no need for any other mechanisms. Therefore, TG is compared separately with others. It shows the order of mechanisms in terms of average power and PDP in voltage range from 0.6 to 2 V. If the concentration is on delay consumption, the right chart can be useful also shows the PDP details for different mechanisms. The methodology

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puts emphasis on doing all the steps in a completely systematic way. It also enjoys high flexibility in design target, while it follows the same procedure to obtain the state-of-the-art designs. This brief has favored SCDM with the wise selection of the circuit components for the PDP target. In the end, three new high performance three-input XOR/XNOR circuits with less PDP and occupied area are conceived using SCDM. The new circuits enjoy higher driving capability, transistor density, noise immunity with low-voltage operation, and the least probability to produce glitches. As a unique feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay.

IV. SCALING AND MULTI VOLTAGE LOGIC

A. Quadded Transistor

The defect-tolerant techniques which are designed to work properly despite the presence of defects, defect avoidance techniques are based on a different principle. That are based on the identification of defective modules and replacing them by other redundant modules through configuration. An approach to nanosystem design is based on a large reconfigurable grid of nanoblocks, each of which can be configured as one of the basic logic building blocks like an AND, an OR, an XOR, half-adder. In the quadded-transistor structure, each transistor A is replaced by four transistors are implemented. Thus implementing the logic (A+A)(A+A) as shown in Figure 1. In order to tolerate single defective transistors, each transistor, A, is replaced by a quadded-transistor structure implementing either the logic function (A+A)(A+A) or the logic functions (AA)+(AA), are shown in fig 1.

In both of the quadded-transistor structures shown in Figure1 (b) & (c), any single transistor defect (stuck-open or stuck-short) will not change the logic behavior, and hence the defect is tolerated.

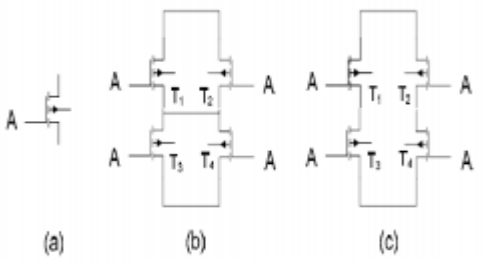

Fig1 (a) Transistor in original gate implementation, (b) First quadded transistor structure, (c) Second quadded transistor structure.

Furthermore, double stuck-open defects are tolerated as long as they do not occur in any two parallel transistors (T1&T2 or T3&T4 for the structure in Figure 3(b), and T1&T2, T1&T4, T3&T2 or T3&T4 for the structure in Figure 3(c)). Double stuck-short defects are tolerated as long as they do not occur in any two series transistors (T1&T3, T1&T4, T2&T3 or T2&T4 for the structure in Figure 3(b), and T1&T3 or T2&T4 for the structure in Figure 3.1(c)). In addition, any triple defect that does not include two parallel stuck open transistors or two series stuck-short transistors is tolerated. Thus, one can easily see that using either of the quadded-transistor structures, the reliability of gate implementation is significantly improved. It should be observed that the effective resistance of the quadded-transistor structures has the same resistance as the original transistor. However, in the presence of a single defect, the worst case effective resistance of the first quadded-transistor structure (Figure 3.1(b)) is 1.5R while that of the second quaddedtransistor structure (Figure 3.1(c)) is 2R, where R is the effective resistance of a transistor. This occurs in the case of single stuck-open defects. For 16 tolerable multiple defects, the worst case effective resistance of both structures is 2R.

B. Scaling

The two main sources of power dissipation in CMOS circuits are static current, which results from resistive paths between power supply and ground, and dynamic power, which results from switching capacitive loads between different voltage levels. There is a third source of power dissipation in CMOS circuits, short-circuit current, which results from both transistors in a CMOS inverter being on at the same time while the input switches. The short-circuit component is small. In addition to Quadded transistor, Scaling Technology is proposed to reduce power dissipation. Scaling rate is approximately 13% / year, halving every 5 years. The size of the circuits also continues to increase. Besides increasing the number of devices, scaling has had a profound impact on both speed and power. In modern SoC designs, different blocks have different performance objectives and constraints. Using above concept; more recent and aggressive approaches to reducing power are: – Power Gating and Adaptive Voltage Scaling. • In the Multi-Voltage design method, the internal logic of the chip is partitioned into multiple voltage regions or power domains, each with its own supply. In RAM circuits we can envision a low voltage to maintain memory contents is not being accessed, and a higher voltage that supports reads and writes. There two types of Scaling.

- Full Scaling (Constant Field Scaling).
- Constant Voltage Scaling.

C. Full Scaling

Full scaling is that scaling which preserves the magnitude of the electric field inside the MOSFET while the dimensions are scaled by a factor S. Due to this scaling technique, the charge densities are advanced by S in order to maintain the magnitude of the fields inside. Say for the scaling factor, S=α, the following observations that influence of full scaling on the current voltage characteristics of MOS transistors,

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make an assumption that the surface mobility, is not significantly affected by the scaled doping density. Before scaling, the instantaneous power dissipated by the MOSFET will be

$$P = I_D V_{DS}$$

Noticing that both of the drain current and drain to source voltage are reduced by a factor S, and then the power also gets by S2. This reduction in power dissipated is a very attractive feature of full scaling. Find that the power density per unit area remains virtually unchanged for the scaled device. Charging & discharging of the capacitance in the MOSFET eventually affects the transient operation of it. Since it is scaled down by a factor S, the charge-up and charge-down time from the transient characteristics of the device after scaling get improved accordingly. This proportional reduction of on-chip dimensions, improves the overall performance by decreasing the parasitic capacitances as well as resistances. The table shown summarizes the changes in scaled-device characteristics as a result of full (constant-field) scaling.

D. Constant-Voltage Scaling

In particular, the peripheral and interface circuitry may require certain voltage level for input and output voltages, which in turn will necessitates multiple power supply voltages and complicated level-shifter arrangements. So, this practically leads constant-field scaling. As done in full scaling, here too the dimensions of the MOSFET are reduced by S. but on the other hand, power supply and power density remains unchanged. Constant voltage scaling of MOSFET dimensions , potentials & doping densities are as shown. Finally, the power density is found to be increased by a factor of S3 after the constant voltage scaling, accompanying with possible adverse on the device reliability. Table beneath shows the effect of constant-voltage scaling in the key device characteristics. As constant-voltage scaling is a disaster for the device reliability, but still it's preferred over full (constantfield) scaling in many practical cases because of the external voltage level constraints. However, it must be known that constant voltage scaling elevates the drain current density and power density by S3, which may cause problems, as, electro migration, hot-carrier degradation, oxide breakdown and electrical overstress in the scaled MOS transistor. As device dimensions are systematically reduced through full scaling, various physical limitations become increasingly more prominent, and ultimately restrict the amount of feasible scaling for some device dimension. The approaches to voltage scaling are:

- Static Voltage Scaling (SVS).
- Multi-level Voltage Scaling (MVS).
- Adaptive Voltage Scaling (AVS).
- Dynamic Voltage and Frequency Scaling (DVFS).

E. Dynamic Voltage and Frequency Scaling

An extension of MVS where a larger number of voltage levels are dynamically switched Switching Times and Algorithms: Switching performance levels take time for both voltage regulators and clock generators. Switching voltage levels is particular slow and switching frequencies is orders of magnitude faster than voltage level switching. Increase the voltage first and decrease the voltage after the frequency is lowered between to follow changing workloads. DVFS is used to save the energy only when the system level performance requirements are understood and it is clear when the frequency can be lowered. For embedded system with a known workload, we can instrument the embedded firmware or hardware to drive the performance request and hence voltage requirements directly.

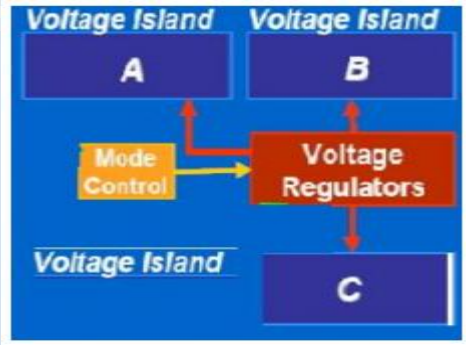

Fig 2 Dynamic voltage and frequency scaling

For a real-time system, the deadlines are well understood and expressed in terms of scheduler priorities or scheduled events. The real-time requirements can be used to drive the performance and voltage scaling hardware. Simply tried to guess from system utilization metrics or statistics is not a good solution. Good example, ARM's Intelligent Energy Manager (IEM). It builds an awareness of producer and consumer task frequencies and deadlines. E.g. for GUI, the calls to the window server and the perceived display refresh rates may be used to judge the right level of performance for interactive tasks.

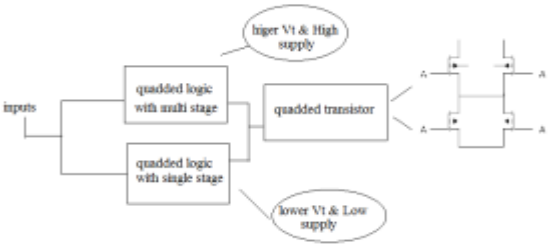

Fig 3 Proposed QLQT with MVL

Thus reducing supply voltage to reduce power dissipation in our quadded logic selectively decrease supply voltage which correspond to fast paths and finish computation early.First the circuit is tested for fault existence if there is a fault is identified then it used Quadded logic technique. By using Quadded logic technique, fault in a circuit is tolerated but power dissipation and delay of circuit is increased. Here multi supply voltage logic is proposed in fast and slow path

thus speed of the circuit increased by reducing the delay on that path. DVFS is introduced and used to save the energy only when the system level performance requirements are understood and it is clear when the frequency can be lowered. For embedded system with a known workload, we can instrument the embedded firmware or hardware to drive the performance request and hence voltage requirements directly.

V. QUADDED LOGIC WITH QUADDED TRANSISTOR

Advances in CMOS technology have made digital circuits and systems very sensitive to manufacturing variations, aging, and/or soft errors. Fault-tolerant techniques using hardware redundancy have been extensively investigated for improving reliability. Quadded logic (QL) is an interwoven redundant logic technique that corrects errors by switching them from critical to subcritical status; however, QL cannot correct errors in the last one or two layers of a circuit. In contrast to QL, quadded transistor (QT) corrects errors while performing the function of a circuit. In this brief, a technique that combines QL with QT is proposed to take advantage of both techniques. The proposed quadded logic with quadded transistor (QLQT) technique is evaluated and compared with other fault-tolerant techniques, such as triple modular redundancy and triple interwoven redundancy, using stochastic computational models. Simulation results show that QLQT has a better reliability than the other fault-tolerant techniques (except in the very restrictive case of small circuits with low gate error rates and very short paths from primary inputs to primary outputs). These results provide a new insight for implementing efficient fault tolerant techniques in the design of reliable circuits and systems. In QLQT, any single error in the second-to-last layer of gates or in the last layer of transistors can be corrected by the QT circuits at the outputs. This provides a significant advantage over QL. However, a critical error at the third last layer that would be corrected in QL, may not be necessarily corrected in a QLQT circuit; this is caused by the fan-outs of the subcritical errors induced at the second last layer onto the last QT structures. However, these errors may not cause an erroneous output due to: 1) the errors may propagate to two transistors that are not in parallel in QT; and 2) the errors may be corrected by other signals due to their subcritical nature. Therefore, the negative effects of QLQT are rather limited. It shows a comparison between QL and QLQT for the effects of single errors at different layers. This brief has a novel fault-tolerant technique that uses both QL and QTs. In the QLQT technique, QTs are implemented at the last layer of a circuit, whereas the remaining circuit is implemented by QL. Simulations have shown that the QLQT technique improves QL by using QTs to implement functions of both the output gates and voters. The fault-tolerant QT circuits correct faults that occur in the last two logic layers, hence leading to a better reliability. Extensive simulations reveal insights with respect to the features and application scopes of these fault-tolerant technique for reliable circuit and system design.

A.DVS ALGORITHMS

Dynamic voltage scaling has been a key technique for exploiting the hardware characteristics of processors to reduce energy dissipation by lowering the supply voltage and operating frequency. The DVS algorithms are shown to make dramatic energy savings while providing the necessary peak computation power in general purpose systems.

VI.CONCLUSION

SCDM serves as a design methodology for three-input XOR/XNOR,which is one of the most complex and competitive as well as all-purpose three-input basic gates in arithmetic circuits. This brief has proposed a novel faulttolerant technique that uses both QL and QT to implement xor and xnor gates . Simulations have shown that the proposed Technique improves both reliability and power minimization. The fault-tolerant QT circuits correct faults that occur in the last two logic layers, hence leading to a better reliability. Extensive simulations reveal insights with respect to the features and application scopes of these fault-tolerant technique for reliable circuit and system design.

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