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DESIGN AND IMPLEMENTATION OF BIST TECHNIQUE WITH UART INTERFACED

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Abstract: Testing is the most prominent role in chip manufacturing unit. The most prominent and present date advanced device for testing would be BIST. BIST may be a style technique that enables a system to check mechanically itself with slightly larger system size. During this paper, the simulation result performance achieved by BIST enabled UART design through VHDL programming is enough to compensate the additional hardware required in BIST design. this system generate random check pattern exploitation the LFSR checks Pattern Generator mechanically, therefore it will offer less check time compared to associate degree outwardly applied check pattern and helps to attain rather more productivity at the top modules. This mechanism also to be used to check the design chip itself. So the main advantage of this testing is that it reduces the complexness thereby will increase the operational speed, potency in conjunction with relevant price reduction. Also in this method the conjunction with operation, maintenance of the system may also be done.

Index Terms— BIST, LFSR, UART, VLSI.

I.INTRODUCTION

Testing of integrated circuits (ICs) is of crucial importance to confirm a high level of quality in product practicality in each commercially and in camera made merchandise. The impact of testing affects areas of producing also as those concerned in style. This want to realize a top quality level should be tempered with the value and time concerned during this method. In VLSI we've testing issues like input combinatorial issues, gate to I/O pin magnitude relation issues, take a look at generation issues, light-emitting diode the designer to spot reliable take a look at ways and solve this issues.teh insertion of special take a look at electronic equipment on the VLSI circuits that enables economical take a look at ways. This has been self-addressed by the requirement for style for testability (DFT) and thus the requirement for BIST. It tests the circuit or system performs itself thus it's named as “self-test". BIST is AN on-chip take a look at logic that's utilized to check the useful logic of a chip, by it. Thanks to the speedy increase within the style quality, BIST has become a serious style thought in DFT ways and is changing into progressively vital in today’s state of the art SoCs. A properly designed BIST is in a position to offset the value of additional take a look at hardware whereas at identical time making certain the dependability, reduces maintenance value and testability. In parallel communication the value still as quality of the system will increase because of concurrent transmission of data bits on multiple wires. Serial communication alleviates this downside and emerges as effective technique in several applications for long distance communication because it reduces the signal distortion attributable to its straightforward structure. Universal Asynchronous Receiver Transmitter (UART) may be a kind of serial communication protocol. The Universal Asynchronous Receiver Transmitter (UART) may be a fashionable and widely-used device for digital communication within the field of telecommunication. Its several blessings like simple resources, reliable performance, robust anti jamming capability, straightforward to work and notice so on The UART may be a giant scale computer circuit that contains all the software system programming necessary to completely control the port of a laptop (Personnel computer).

II. BIST TECHNIQUE

VLSI testing problems like Test generation problems, input combinatorial problems, gate to I/O pin ratio problems are discussed [3] and this motivated designers to identify reliable test methods in solving these difficulties. An insertion of special test circuitry on the VLSI circuit that allows efficient test coverage is the answer to the matter .This has been addressed by the need for design for testability (DFT) and hence the need for BIST. BIST is an on-chip test logic that is utilized to test the functional logic of a chip, by itself. Fig. 1shows a BIST module composition.

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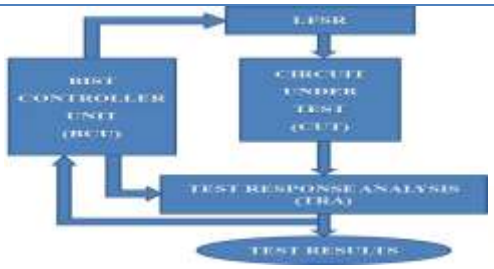

Fig 1:Generic BIST architecture

III. LITERATURE SURVEY

Most microprocessor in today's market is based on either RISC or CISC architecture technologies. The RISC architecture boost the computer speed also used in control algorithms .Using of RISC Processor the time required to execute each instruction can be shortened and the number of cycles reduces. In [1] paper depicts a RISC building design in which 2 cycle operation is gotten utilizing a pipelined outline. The pipelined architecture is used which minimizes the latency and increases the speed and in the new innovation the 2 stage pipelining which works on the positive edge and as well as in the negative edge minimizes the latency and increases the speed and also reduce the stalling in instruction. The whole architecture of RISC processor work on the 2 cycle .the fixed size of instruction allows the given instruction to be easily piped. RISC processor has a flexible architecture. In [2] the second approach clock gating technique is used to minimize the Power. This is a most Popular method to reduce the dynamic Power consumption. Power is devoured by the combinational rationale whose qualities are changing on each one clock edge so the gating rationale comes into the Picture and clock is turned off. In the present research work , the outline of 16 bit RISC processor is introduced implemented for high efficiency and low power. The architecture supports 33 instructions. The instruction cycle consist of 2 stage pipelining and perform fetch, decode, execute, write back operation simultaneously. The control unit Generate signals from the given instructions. The architecture supports arithmetic, logical, shifting and rotation operations. In [3] this approach proposed RISC processor based on MIPS designed here is an effort towards efficient processor suitable for various applications. CISC processors have received the marketplace over the years. They support various addressing modes and various data types like others complex processors. Length of instruction varies from instruction to instruction. They generally access data from external memory. They are basically implemented using micro programmed control. There is little gap between instructions of CISC processor and higher-level language statements. However, they may save memory space, its design is complicated and instructions are variable in length; special hardware is required for boundary marking of instruction. After an deep study it is proved that simple instructions has been used 80% of the time and complex instructions has been replaced by group of simple instructions. In [4] this approach a lot many new amount of Processor's are also into the market. Out of all these processor's a few of them were designed using processor cores i.e. Hardware Description Languages like Verilog-HDL and VHDL (Very High Speed Integrated Circuit Hardware Description Language) , is used for writing a particular version of processor. This helps the designer to use them in any of the embedded applications. These can be used in the processor just by embedding a particular application in the processor. RISC (Reduced Instruction Set Computer) is an efficient Computer Architecture which can be used for the Low power and high speed applications of the processor RISC Processors are important in application of pipelining. The curb of the processor is the Instruction Set Architecture used for developing it. The total worthiness of the processor depends on utilizing the Instruction Set Architecture. Instruction Set Architecture is a metaphysical interface between Low level system of the machine and the hardware, that contain all the information about the machine , required to However a lot of research is being carried out in the field of processor's to satisfy the performance issues. But now a days it is mandatory to use a machine which is efficient in the terms of speed, power, performance and size. Though there are tradeoffs between all the performance parameter's, Research is being carried out to satisfy all the above performance parameters. Though a more number of instruction sets are available in the market, an instruction set which can handle less power, high speed low area needs to be selected for the efficient functioning. To satisfy all the above requirements we consider the MIPS (Microprocessor without Interlocked Pipelining Stages) Instruction Set Architecture. This paper also concentrates on reducing the power utilized by the processor in order to satisfy the Low Power constraint of the developed Processor.

IV. PROPOSED METHOD

In this paper, we proposed a novel architecture which generates the test patterns with reduced switching activities. LP-TPG structure consists of modified low power linear feedback shift register (LPLFSR), m-bit counter, gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates 2m test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next seed. The seed generated from LP-LFSR is Exclusive–ORed with the data generated from gray code generator. The patterns

generated from the Exclusive–OR array are the final output patterns.

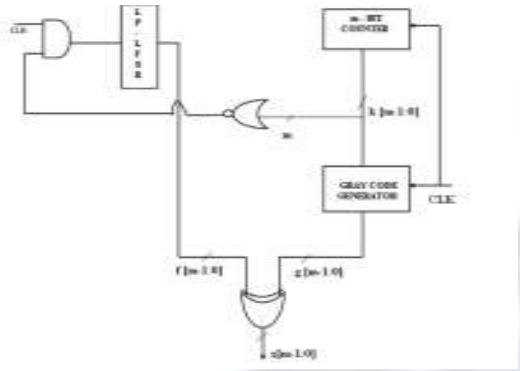

Figure 2. Low Power Test Pattern Generator

V. ALGORITHM FOR LP-LFSR

The algorithm for LP-LFSR is given below: Consider a N-bit external (or) internal linear feedback shift register [n>2].

- For example n-bit, external LFSR is taken, which consists of n-flip flops in series. A common clock signal is applied as control signal for all flip flop.
- For exchanging the output of adjacent flip flops, multiplexers are used. The output of the last stage flip flop is taken as a select line.
- If the last stage flip flop output is one, any one of the flip flop output is swapped with its adjacent flip flop output value.
- If the last stage flip flop output is Zero, no swapping will be carried out. The output from other flip flops will be taken as such.
- If the LFSR is moved through a complete cycle of 2n states then the transitions expected are 2n-1.When the output of the adjacent flip flops are swapped, the expected transitions are 2n-2.Thus the transitions produced are reduced by 50% compared with original LFSR. The transition reduction is concentrated mainly on any one of the multiplexer output.
- Gray converter modifies the counter output such that two successive values of its output are differing in only one bit. Gray converters can be implemented as shown below.

g[n-1]= k [n-1]
g[n-2]= k [n-1] XOR k[n-2] . .
g[2]= k [2] XOR k[3] 3336
g[1]= k[1] XOR k[2]
g[0]= k[0] XOR k[1]

In [12] it is stated that that the conventional LFSR's outputs cannot be taken as the seed directly, because some seeds may share the same vectors. Thus the LP-LFSR should ensure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. Test patterns generated from the proposed structure are implemented as following equations.

x[0] = f[0] XOR g[0]
x[1] = f[1] XOR g[1]
x[2] = f[2] XOR g[2]
x[3] = f[3] XOR g[3]
x[4] = f[4] XOR g[4]
x[5] = f[5] XOR g[5] . .. X [n-1] = f[n-1] XOR g[n-1]

Thus the XOR result of the sequences is single input changing sequence. In turn reduces the switching activity and so power dissipation is very less compared with conventional LFSR.

Fig. 2 is an example of counter and its respective gray value. It is shown that all values of g[2:0] are single input changing patterns. Patterns:

K [2:0] g [2:0]
K0= 000 g0= 000
K1= 001 g1= 001
K2= 010 g2= 011
K3= 011 g3= 010
K4= 100 g4= 110
K5= 101 g5= 111
K6= 110 g6= 101
K7= 111 g7= 100

V. UART TRANSMITTER

UART transmitter module consists of output register, an transmitter buffer register and transmitter controller logic i/o pins are:

• TxD is the port for serial data output
• TxC bar is the transmitter clock input
• TxE is the transmitter control logic
• ACK & RST are two control inputs

C. Transmit Module

The function of transmit module is to convert the sending8-bit parallel data into serial data, adds start bit at the head of the data as well as the parity and stop bits at the end of the data. When the UART transmit module is reset by the reset signal, the transmit module immediately enters the ready stateto send. In this state, the 8-bit parallel data is read into the register txdbuf [7: 0]. The transmitter only needs to output 1 bit every 16 bclkt (the transmitting clock frequency generated bythe baud rate generator) cycles. The order follows 1 start bit, 8data bits, 1 parity bit and 1 stop bit. The parity bit is determine according to the number of logic 1 in 8 data bits. Then the parity bit is output. Finally, logic 1 is output as the stop bit

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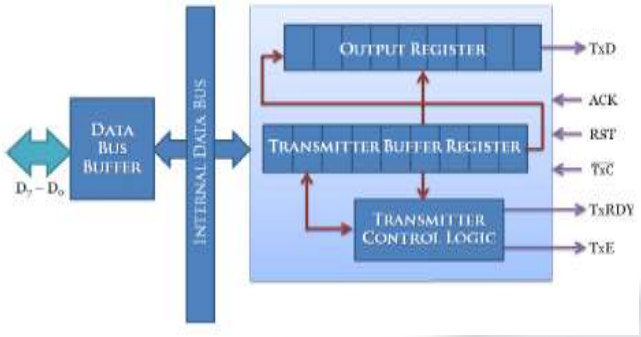

Fig. 3: UART Transmitter

VI. UART RECEIVER

The architecture of UART receiver section. The followings are the brief description of each block **Input Register**: I/P register is a serial input and serial output register which consists of 8 D-flip flops to store and shift 8 bit input data. The input data of the register is the serially transmitted data from the transmitter.

Receiver buffer register: It is a 8 bit serial in parallel out register. The data of i/p register is shifted and enters bit by bit in every rising clock edge in Receiver Buffer Register. After entering 8 bit data, the buffer gets full.

Receiver Control Logic: This block decides when data is tobe taken inside the receiver and when data is to be sent to peripheral device.

1) When the peripheral device wants data from the receiver and the receiver buffer register is full simultaneously, then receiver buffer register data are sent to the peripheral device.

2) When the peripheral device does not want data from the receiver but the receiver buffer register is full then any data cannot be taken inside the Receiver section and if any data arrives then data should be discarded.

3) When the peripheral device want data from the receiver but the receiver buffer register is not full then no data is send to the peripheral and data is taken in Receiver buffer from the register.

4) When the peripheral device does not want data from the receiver and the receiver buffer register is not full then data is taken inside Receiver buffer from input register with each clock pulse rising but data is not sent to the peripheral

During the UART reception, the serial data and the receiving clock are asynchronous, so it is very important to correctly determine the start bit of a frame data. The receive module receives data from RXD pin. RXD jumps into logic 0from logic 1 can be regarded as the beginning of a data frame. When the UART receiver module is reset, it has been waiting the RXD level to jump. The start bit is identified by detecting RXD level changes from high to low. In order to avoid the misjudgment of the start bit caused by noise, a start bit error detect function is added in this design, which requires the received low level in RXD at least over 50% of the baud rate to be able to determine the start bit arrives. Since the receive clock frequency is 16 times the baud rate in the design, theRXD low level lasts at least 8 receiving clock cycles is considered start bit arrives. Once the start bit been identified ,from the next bit, begin to count the rising edge of the baud clock, and sample RXD when counting. Each sampled value of the logic level is deposited in the register rbuf [7, 0] by order.

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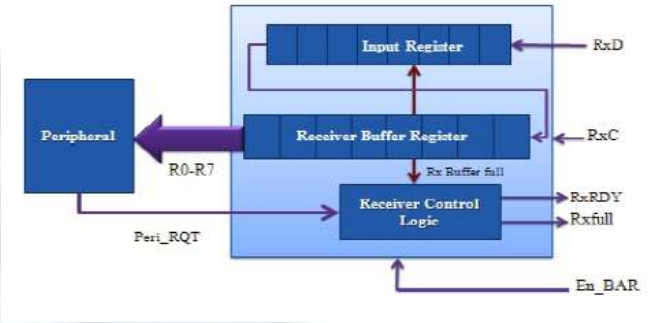

Fig. 4: UART Receiver

VII. SIMULATION RESULTS

The verilog HDL coding and simulation of the design are done in Xilinx tool ISim 14.4. The operating clock frequency used for simulation is 50 MHz. The baud rate set is 9600bps. Data word length is 8-bits.

A. Simulation Results of Transmitter

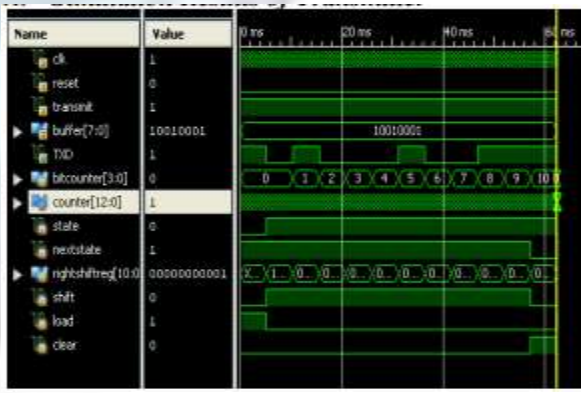

Fig 5: UART tramsmitter

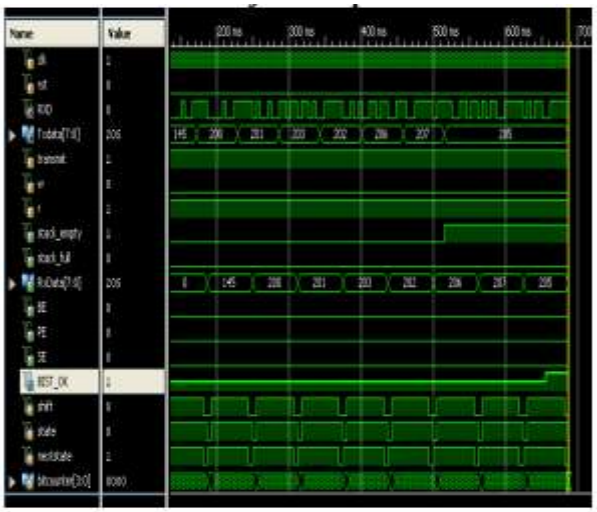

Fig 6: output of bist interfaced with uart

VIII. CONCLUSION

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is Ex-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator.

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