IPHV8I2042X
International Journal Of Advanced Research and Innovation -Vol.8, Issue .II
ISSN Online: 2319 – 9253
Print: 2319 – 9245

DESIGN AND IMPLEMENTATION OF REVERSE CONVERTER DESIGN VIA PARALLEL-PREFIX ADDERS

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ABSTRACT: In this brief, the implementation of residue number system reverse converters based on well-known regular and modular parallel prefix adders is analyzed. The VLSI implementation results show a significant delay reduction and area × time2 improvements, all this at the cost of higher power consumption, which is the main reason preventing the use of parallel-prefix adders to achieve high-speed reverse converters in nowadays systems. Hence, to solve the high power consumption problem, novel specific hybrid parallel-prefix-based adder components that provide better tradeoff between delay and power consumption are herein presented to design reverse converters. A methodology is also described to design reverse converters based on different kinds of prefix adders. This methodology helps the designer to adjust the performance of the reverse converter based on the target application and existing constraints.

Key Terms— Digital arithmetic, parallel-prefix adder, residue number system (RNS), reverse converter.

I.INTRODUCTION

In the world of battery-based and portable devices, the residue number system (RNS) can play a significant role due to its low-power features and competitive delay. The RNS can provide carry-free and fully parallel arithmetic operations [1], [2] for several applications, including digital signal processing and cryptography [3]–[6]. However, its real usage requires forward and reverse converters to be integrated in the existing digital systems. The reverse conversion, i.e., residue to binary conversion, is a hard and time-consuming operation [7]. Hence, the problem of designing high-performance reverse converters has motivated continuous research using two main approaches to improve the performance of the converters: 1) investigate new algorithms and novel arithmetic formulations to achieve simplified conversion formulas and 2) introduce new module sets, which can lead to more simple formulations. Thereafter, given the final simplified conversion equations, they are computed using well-known adder architectures, such as carry-save adders (CSAs) and ripple-carry architectures, to implement carry-propagate adders (CPAs) and, more seldom, fast and expensive adders such as the ones with carry-look ahead or parallel-prefix architectures. In this brief, for the first time, we present a comprehensive methodology to wisely employ parallel-prefix adders in carefully selected positions in order to design fast reverse converters. The collected experimental results based on area, delay, and power consumption show that, as expected, the usage of the parallel-prefix adders to implement converters highly increases the speed at the expense of additional area and remarkable increase of power consumption. The significant growing of power consumption makes the reverse converter not competitive. Two power-efficient and low-area hybrid parallel-prefix adders are presented in this brief to tackle with these performance limitations, leading to significant reduction of the power delay product (PDP) metric and considerable improvements in the area-time2 product (AT2) in comparison with the original converters without using parallel-prefix adders.

Residue number system is having a great influence on all digital systems due to its low power features and the modest delay[]. Residue number system is a non-weighted integer number representation and uses the residues of numbers in specific modulus for its representation [2]. The residue number arithmetic operations are implemented in parallel and that are nearly carry free. The residue number system is usually employed in applications like digital signal processing, image processing and cryptography [3]. The absence of the carry propagation leads to high speed processing in the RNS based applications. Using RNS representation, larger number is encrypted into smaller numbers. Residue number system reduces the complexity of the individual arithmetic blocks. This results in reduction in power. The residue number system is a non-weighted number system with no dependency between its channels. Thus, an error in one channel does not transmit to the other channels. RNS has less possibility of errors. Residue number system can be used for reduction in supply voltage, compared to the binary structural design. But division, square-root, sign detection, and magnitude comparison are very difficult operations in the residue number system. The

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forward converter, arithmetic unit and reverse converters are the main parts of the residue number system. The forward converter performs the binary to residue conversion while the reverse converter performs the operation of reverse converting the residue to binary number. In contrast to other parts reverse converter have the more complex and non-modular structure. So the process of reverse converting is tough and time consuming process. Therefore more care should be given to its design in order to avert slow operation and without compromising the benefits of RNS. In reverse converter design the value of moduli of the moduli set must be substituted in conversion algorithm formulas obtained from Chinese remainder theorem (CRT) [5], mixed radix conversion (MRC) [4], and new Chinese remainder theorem. The final equation from conversion theorem should be simplified by using some properties and the final binary representation is recognized using the adder. Usually the design of the reverse converters is done using the parallel prefix adders for higher speed operation. But it suffers from higher power consumption. The parallel prefix adders are more flexible and used to increase the speed in binary additions.

II.NEW PARALLEL-PREFIX-BASED COMPONENTS

The Chinese remainder theorem, or other related improved approaches and techniques [7] underlie the RNS reverse conversion, whose formulation can be directly mapped to ripple-carry adders (RCA). However, this leads to significant speed degradation, due to the linear increase of the delay in the RCA with the number of bits. Parallel-prefix adders can be used in the RNS reverse converters to bind the delay to logarithmic growth. However, in reverse converters, several parallel-prefix adders are usually required. Even when only one adder is used, the bit length of this adder is quite large. Consequently, this results in high power consumption notwithstanding its high speed. Therefore, in this section, two approaches that take advantage of the delay properties of the parallel prefix adders with competitive power consumption are introduced. Usually, one regular binary addition is required in reverse converter structures to achieve the final binary representation. This final addition has an important effect in the total delay of the converter due to the large bit-length of the operands. A thorough assessment of this final regular addition in recent converter designs shows that one of the operands has some constant bits with value 1 as highlighted by the following lemma, which applies to a class of converters described in [10].

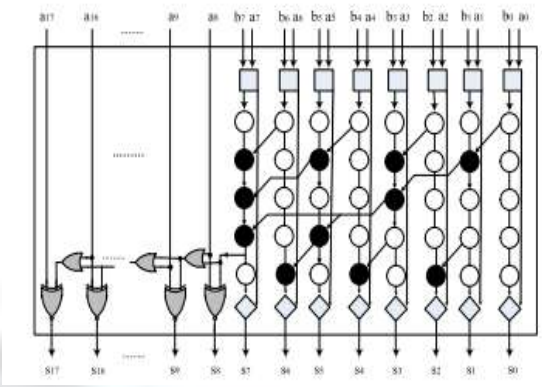

Fig. 1. HRPX structure with BK prefix network.

Lemma 1: (2n + 1) bits of the second operand of CPA4 of the converter in [10] are always constant and equal to one's.

Proof: The [10, CPA4] is a (4n + 1)-bit regular RCA that performs the subtraction presented in [10, eq. (52)]. This subtraction is accomplished in [10] as follows: The parallel prefix structures will provide a higher speed for the reverse converters and it is flexible [1]. The Parallel prefix structure consists of three main blocks, they are preprocessing block, prefix carry tree and post processing block.

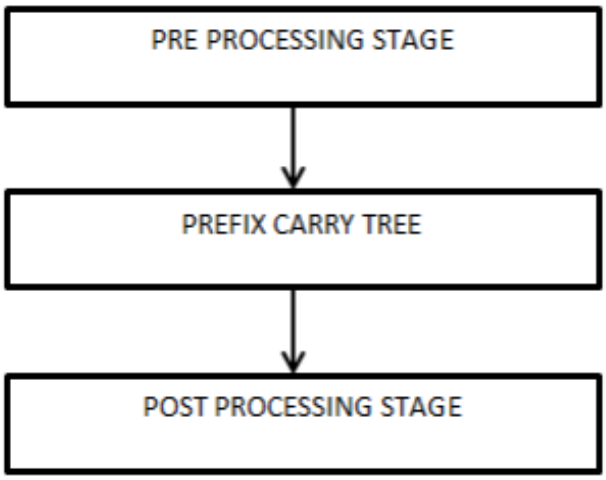

Fig.1.parallel prefix structure

The figure.1 shows the three stages of the parallel prefix structure. The parallel prefix adder operation begins with preprocessing stage by generating the Generate (Gi) and Propagate (Pi) signal equations. The prefix carry tree get proceeded with the previous block signal to yield all carry bit signal and these stage contains three logic complex cells such as Black cell, Grey cell and Buffer cell. Black cell compute both propagate and generate of previous two blocks (right and the left block). The Grey cell executes only the generate bit and carry is generated. The carry bits generated in the second stage get passed to the post processing block thereby generating the sum. The converter design via parallel prefix adder structure alone will increase the speed of the converters at a cost of higher power consumption. Thus a hybrid parallel prefix adder structure is introduced. Specific hybrid parallel prefix adder components like hybrid regular parallel prefix XOR/OR(HRPX) adder

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for (4n+1) bit addition and hybrid modular parallel-prefix excess-one (HMPE) adder for (2n-1) modulo addition is used to replace the existing adder components. 1-HRPX Structure (Hybrid Regular Parallel prefix XOR/OR adder component) HRPX structure with the BK-KS prefix structure is used to perform the addition. The regular parallel prefix adder is used to do the first part of addition and the simplified RCA logic is used to do the second part where the corresponding bits of the operand are fully variable. Full adder can be designed with XOR/OR gates because of the constant operand. In these reverse converters design the carry chain is not needed and can be ignored.

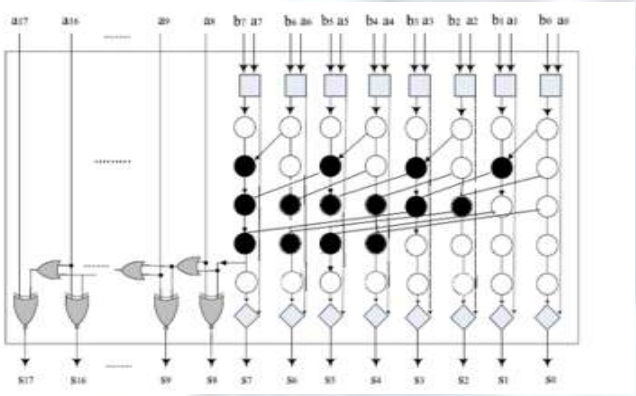

Fig.2. HRPX Structure

The modulo 2n − 1 addition is an essential operation in the reverse conversion for most moduli sets. The regular CPA with end around carry (EAC) is by default a moduli 2n − 1 adder with double representation of zero, but in reverse converters a single representation of zero is required. So, a detector circuit has to be used to correct the result, which imposes an additional delay. However, there is a binary-toexcess-one converter, which can be modified to fix the double representation of zero issue. 2-HMPE Structure (Hybrid Modular Parallel prefix Excess one adder component) However, we could address the problem of power consumption by eliminating the additional prefix level and using a modified excess-one unit instead. In contrast to the BEC, this modified unit is able to perform a conditional increment based on control signals.

The HMPE consists of two parts:

1) A regular prefix adder

2) A modified excess-one unit

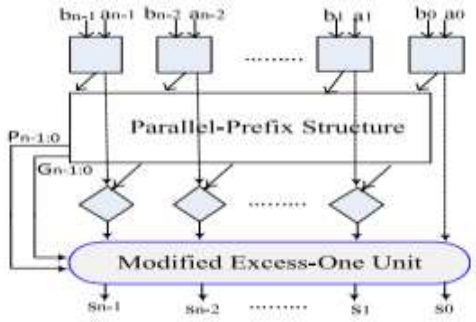

Fig. 3. HMPE structure.

propagating signals at each prefix level. An optimized approach is proposed in [21], which uses an extra prefix level to add the output carry. However, this method suffers from high fan-out, which can make it usable only for small width operands. However, we could address this problem by eliminating the additional prefix level and using a modified excess-one unit instead. In contrast to the BEC, this modified unit is able to perform a conditional increment based on control signals as shown in Fig. 2, and the resulted hybrid modular parallel-prefix excess-one (HMPE) adder is depicted in Fig. 3. The HMPE consists of two parts: 1) a regular prefix adder and 2) a modified excess-one unit. First, two operands are added using the prefix adder, and the result is conditionally incremented afterward based on control signals generated by the prefix section so as to assure the single zero representation. Summarizing, the HMPE is highly flexible, since it can be used with every prefix networks. Hence, the circuit performance metrics such as area, delay, and power-consumption can be adjusted by selecting the desired prefix structure. On the other hand, the HRPX avoids the usage of a large size parallel-prefix adder with high powerconsumption, and also does not have the penalty of using the long carry-propagation chain of a RCA.

III.REVERSE CONVERTER DESIGN METHODOLOGY

In this section, the methodology of reverse converter design is described. In the following, a method employing distinct components in the architecture of the reverse converter will be presented. Several reverse converters for different moduli sets have been introduced, which can be classified into three classes. The first class consists of converters with a tree of CSAs with EAC followed by a two-operand modulo 2k − 1 CPA [8], [10]. A second class includes more complex reverse converters, which have several CSAs and CPAs with EACs followed by a final regular subtractor with two operands of different size [10]–[12]. The implementation of this subtractor using regular binary-adder results in one operand with some constant bits. The third class covers the reverse converters that have been designed for moduli sets with moduli other than the popular 2n and 2n ± 1 [14].

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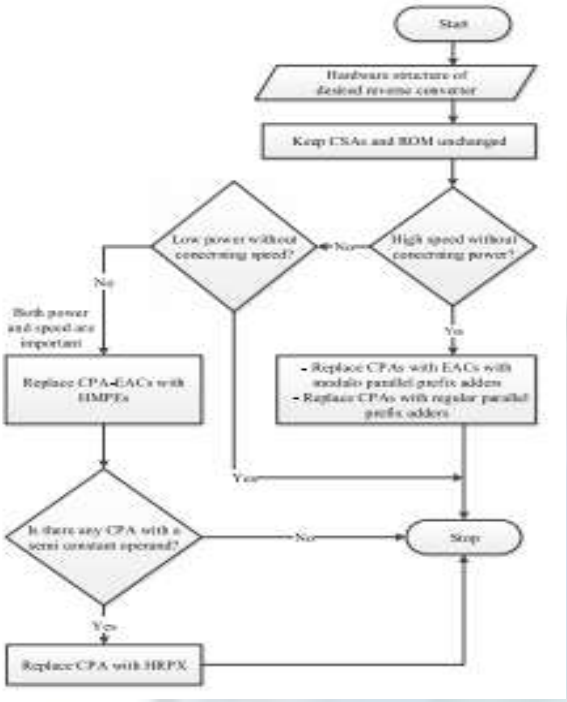

Fig. 4. Reverse converter design methodology.

In the following, we describe a methodology for designing reverse converters in the first and second classes. The suggested method for applying the HMPE and HRPX in the reverse converter is shown in Fig. 4. First of all, it is relevant to decide about the required performance metrics based on the specified application. If it is just important to achieve the least power consumption and hardware cost without considering speed, no prefix adder is needed. On the other hand, if high speed is the designer goal, the CPAs with EAC and the regular CPAs should be replaced by traditional parallel prefix modulo 2n − 1 adders and regular parallel-prefix adders, respectively. However, for the VLSI designers, a suitable tradeoff between speed, power, and area is often more important. In this case, first, CPAs with the EAC can be replaced by the HMPEs. Then, if the converter contains a regular CPA where one of its operands has a string of constant bits with the value of one, it can be replaced with the HRPX.

1. Output waveforms

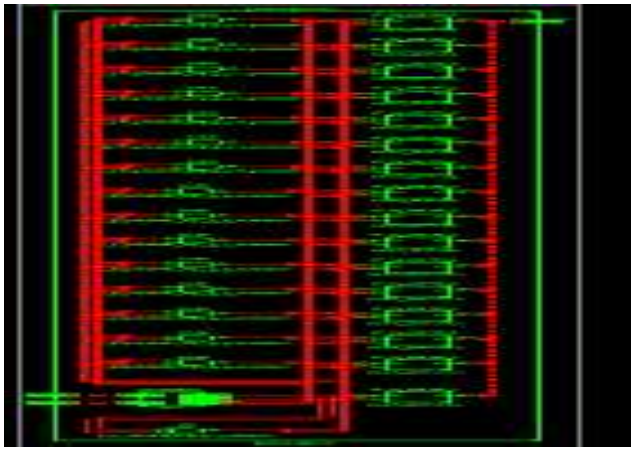

Fig 5: rtl schematic of the circuit

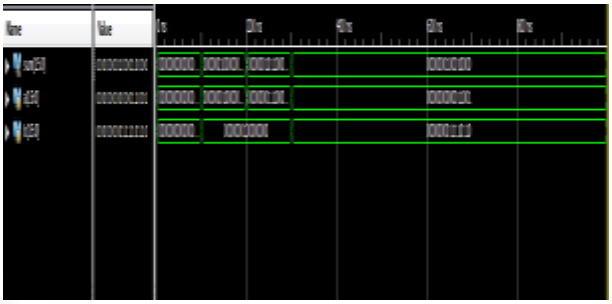

Fig 6:output waveform

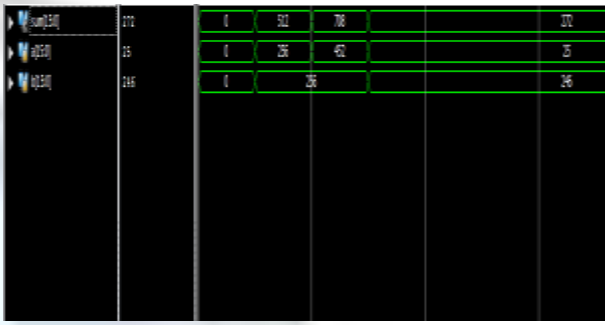

Fig 7:output waveform 2

V.CONCLUSION

This brief presents a method that can be applied to most of the current reverse converter architectures to enhance their performance and adjust the cost/performance to the application specifications. Furthermore, in order to provide the required tradeoffs between performance and cost, new parallel-prefix-based adder components were introduced. These components are specially designed for reverse converters. Implementation results show that the reverse converters based on the suggested components considerably improve the speed when compared with the original converters, which do not use any parallel-prefix adder, and reduce the power consumption compared with the converters that exclusively adopt parallel-prefix adders.

REFERENCES:

[1] A. Omondi and B. Premkumar, Residue Number Systems: Theory and Implementations. London, U.K.: Imperial College Press, 2007.

[2] B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd ed., New York, NY, USA: Oxford Univ. Press, 2010.

[3] J. Chen and J. Hu, "Energy-efficient digital signal processing via voltageover scaling-based residue number system," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 7, pp. 1322–1332, Jul. 2013.

[4] C. H. Vun, A. B. Premkumar, and W. Zhang, "A new RNS based DA approach for inner product computation," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 8, pp. 2139–2152, Aug. 2013.

[5] S. Antão and L. Sousa, "The CRNS framework and its application to programmable and reconfigurable cryptography," ACM Trans. Archit. Code Optim., vol. 9, no. 4, p. 33, Jan. 2013.

[6] A. S. Molahosseini, S. Sorouri, and A. A. E. Zarandi, "Research challenges in next-generation residue number system architectures," in Proc. IEEE Int. Conf. Comput. Sci. Educ., Jul. 2012, pp. 1658–1661.

[7] K. Navi, A. S. Molahosseini, and M. Esmaeildoust, "How to teach residue number system to computer scientists and engineers," IEEE Trans. Educ., vol. 54, no. 1, pp. 156–163, Feb. 2011.

[8] Y. Wang, X. Song, M. Aboulhamid, and H. Shen, "Adder based residue to binary numbers converters for (2n − 1, 2n, 2n + 1)," IEEE Trans. Signal Process., vol. 50, no. 7, pp. 1772–1779, Jul. 2002.

[9] B. Cao, C. H. Chang, and T. Srikanthan, "An efficient reverse converter for the 4-moduli set {2n − 1, 2n, 2n + 1, 22n + 1} based on the new Chinese remainder theorem," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 50, no. 10, pp. 1296–1303, Oct. 2003.

[10] A. S. Molahosseini, K. Navi, C. Dadkhah, O. Kavehei, and S. Timarchi, "Efficient reverse converter designs for the new 4-moduli sets {2n − 1, 2n, 2n + 1, 22n+1 − 1} and {2n − 1, 2n + 1, 22n, 22n + 1} based on new CRTs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 823–835, Apr. 2010.

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