IPHV8I3003X
International Journal Of Advanced Research and Innovation -Vol.8, Issue .III
ISSN Online: 2319 – 9253
Print: 2319 – 9245

MEMORY-DECREASED FASTER INTERPRETING STRUCTURE USING NII METRIC COMPRESSION

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ABSTRACT: This short proposes another pressure system of next-emphasis introduction measurements for unwinding the capacity requests of turbo decoders. The proposed conspire stores just the scope of state measurements and also two files of the most extreme and least esteems, while the past pressure strategies need to store the majority of the state measurements for instating the accompanying cycle. We likewise show an equipment amicable recuperation technique, which can be executed by straightforward multiplexing systems. Contrasted with the past work, accordingly, the proposed pressure strategy decreases the required stockpiling bits by 30% while giving the worthy mistake amending execution practically speaking.

Keywords: *Decoding, Bit error rate, Iterative decoding, Turbo codes, Indexes, Optimization, Buffer storage.*

I. INTRODUCTION

Two impact factors for the power consumption of a signal processing circuit can be identified: Power consumption of the logic (roughly related to the algorithmic complexity) and power consumption of the involved buffer memory. The latter is related to the number of read-write operations and their reduction has become a key factor when designing energy efficient algorithms. Especially in state-of-the-art baseband signal processing, where large blocks are often processed in an iterative fashion, memory access is a major power consuming part. At the same time, system on chips (SoCs) are dominated in terms of area by the embedded memory. Given that embedded memories are already highly structured and highly optimized devices, there is less potential for energy optimization if hard quality constraints are reinforced.

However, if relaxing quality requirements in a controlled fashion, significant energy reduction can be achieved: In aggressive voltage scaling (AVS) (Hegde and Shanbhag, 2001; Djahromi et al., 2007; Makhzan et al., 2007), the supply voltage of an embedded circuit is deliberately reduced below the required threshold. This leads to substantial reduction of power consumption, but also to unreliable operation of the circuit. But while the latter would introduce processing errors and serious performance degradation of the whole system if circuit logic was affected, it can be tolerated up to a certain level for some applications in case of embedded memories. This is for example true for baseband signal processing systems, like channel decoders, which are actually designed to deal with error-prone data and can thus be extended to deal with deliberately introduced errors as well. As an example, Hussien et al. (2010) propose an error-resilient Viterbi decoder architecture, where power savings of 15 % to 20 % are achieved while the bit error rate (BER) performance degradation is insignificant.

In context of baseband signal processing and channel decoding, a few authors have addressed a co-design with erroneous circuits under different conditions: The inherent fault-tolerance of communication systems is exploited by Djahromi et al. (2007), where the authors identify a duality between communication channel errors and hardware induced errors. Based on this observation they propose to adapt the supply voltage depending on the current working condition of the system; by reducing the supply voltage in case of good reception conditions they achieve power savings of around 45 % in a WCDMA receiver The resilience of Viterbi and MaxLog decoding against timing errors and memory errors introduced by voltage overscaling is treated in Liu et al. (2009), where power savings of about 44 % and 38 % are reported for Viterbi and MaxLog decoders, respectively.

The authors of Abdallah and Shanbhag (2009) also deal with Viterbi decoding and the influence of timing errors due to process variations and voltage scaling. They investigate several low level methods to improve error resilience and achieve significant power savings of up to 71 % with a small tolerated loss of coding gain. A more abstract treatment of error-resilient Viterbi decoding using an erroneous receive buffer is provided by Hussien et al. (2010), where the authors employ a statistical model of the combined communication channel and hardware noise to derive a suitable branch metric. They also show that the branch metric computation can be kept simple in case of Two's complement representation of the quantization symbols and report a reduction of power consumption in the order of 15 % to 20 % with small loss of coding gain. The authors extend their approach in Hussien et al. (2011) to LDPC and Turbo decoders considering the receive (ARQ) buffer; in Khairy et al. (2012) they also study its application to MIMO detection. For an LDPC decoder Alles et al. (2007); May et al. (2008) propose a reliabilityaware design,

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which improves the protection against timing and signal errors by using simple error correction and detection techniques. Low and high level approaches to improve error-resilience of a Turbo decoder are investigated by Brehm et al. (2012). On algorithm level, the authors propose an increase of iteration number to facilitate resilience against timing errors and soft errors. The same authors also study the resilience of a MIMO-BICM system with iterative receiver and hardware errors that manifest as transient bit errors in various components (Gimmler-Dumont et al., 2012) and conclude that for low error rates, performance of the original system can almost be retained by employing additional iterations. Considering the problem of improving resilience of channel decoding algorithms against memory defects under more general, algorithmic perspective, it is interesting, that only the works by Kurdahi, Eltawil, et al. (Hussien et al., 2010, 2011) consider modification and adaption of the decoding algorithm itself. Furthermore, the strong relation of the given problem to source channel coding and robust quantizer design has only been pointed out in Novak et al. (2010); Roth et al. (2012), while its significance is long known in those fields. Novak et al. (2010) consider a MIMO BICM system with unreliable storage of the received log-likelihood ratio (LLR) values.

The authors investigate the influence of (redundant) index assignments and simple forward error correction codes for the indices in terms of achievable rate and conclude that in case of non-redundant indices the selection of a robust index assignment is crucial, while in case of redundant labels the decision between simple FEC coding and customized index assignment depends on the SNR operation state of the underlying system. The authors address the first point more extensively in Roth et al. (2012) and stress the importance of application specific index assignments. They discuss the cases of repetition coding and convolutional coding and derive optimized index assignments through exhaustive search. For a Turbo decoder with unreliable LLR buffer, an index assignment optimization strategy based on the EXIT characteristics of the decoder is described in Geldmacher and Götze (2013). The authors show that the resulting assignments provide improved error-resilience without increasing decoding complexity. In this article, the influence of optimized index assignment and quantizer design on a Turbo decoder with unreliable receive buffer memory is studied. This scenario of communication channel with quantized output and successive unreliable buffer memory is modeled as a cascade of two discrete memoryless channels (DMCs); the index assignment is regarded as a way to connect both DMCs. It is shown that joint optimization of index assignment and quantizer can significantly improve error-resilience of the decoder, without increasing its computational complexity.

II. PROBLEM DESCRIPTIONS

2.1 System model

The model shown in Fig. 1 is employed to discuss the problem of an unreliable buffer memory. A source generates Gaussian distributed values r˜ from the original equiprobable and independent symbols x ∈ {±1},

r˜ = μrx + n, where n ∼ N (0, σ^2 r). (1)

Figure 1. Model of a Gaussian source with successive quantizer and buffer memory.

The source abstractly models for example an AWGN communication channel, with a certain gain μr and a noise variance σ 2 r , or it may be a so called a priori channel representing a SISO component in an iterative processing system, e.g. a MAP decoder. Given the continuous, Gaussian distributed values r˜, the N-Bit quantizer assigns discrete reconstruction values r from a finite set Q of size |Q| = 2 N in a suitable fashion. In the following the quantizer is designed using uniform and fixed reconstruction values from a set.

Q = {−2 $^{d-1}$ + k2 $^{-f}$: 0 ≤ k < 2 ^{N} }, (2)

where d and f are decimal and fractional bits and d+f = N. This approach is simple and might not include the optimum quantizer design with respect to the mean-squarederror (MSE) or the average mutual information (MI), but it seems practically relevant and enables us to discuss effects of the memory channel disturbance. To account for changing channel conditions (μr and σ 2 r), the scaling factor γ can be used as an adaptive gain control and scale the quantizer input to the quantization range. In some use cases, for example if the source models a constituent decoder in a Turbo decoding framework, the scaler γ might, however, be fixed for practical reasons. Given the set Q, the probability mass function (PMF) P (r|x) of the quantized values r conditioned on x can be found by integrating over the individual quantization intervals.

The quantization scheme coincides with the Two's complement representation, if the assignment from quantization index k to the index i, whose binary representation is stored in the buffer, is selected as i = k ⊕ 2 d−1 with ⊕ denoting the XOR operation and i ∈ {0,... ,2 N−1 }. In general, however, any mapping from quantization values to indices may be used. We refer to this bijective mapping as the index assignment and denote a specific one-to-one relation between k and i by 5, i = 5(k), and its reverse as 5−1 . The binary representation of the integer i is written to the buffer memory. As in Novak et al. (2010); Khajeh et al. (2010), spatially independent and uniformly distributed errors on the memory cells are assumed, such that the memory channel can be seen as a binary symmetric channel

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(BSC) with input and output the binary representations of i and j , respectively. It is referred to as the memory channel in the following. Given the bit error probability pe, the probability of reading an index j under the condition that i has been written to the memory is given as

$$P(j|i) = p^{dH(i,j)} e\,(1-pe)^{N-dH(i,j)} \quad (3)$$

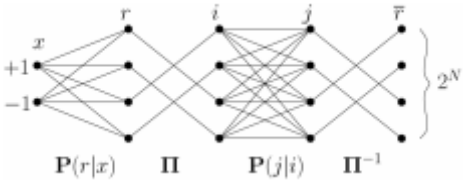

Figure 2. Abstract representation of the AWGN channel with successive quantizer and unreliable buffer memory as DMC cascade.

where dH(i, j) is the Hamming distance between i and j . Given the fact that the index assignment is a bijective mapping, then for the PMF of the reconstructed quantization symbols r ∈ Q conditioned on x it holds that

$$P(r|x) = P(¶^{-1}(j)|x). \quad (4)$$

2.2 Characteristics of memory channel

The transmission matrix (Cover and Thomas, 1991, p. 189) of the AWGN channel with quantized outputs and binary input is a (2×2^N)-matrix and it can be written as

$$\mathbf{P}(r|x) = \begin{bmatrix} P(q_0|-1) & \dots & P(q_{2^N-1}|-1) \\ P(q_0|+1) & \dots & P(q_{2^N-1}|+1) \end{bmatrix}. \quad (5)$$

with qk ∈ Q the reconstruction values of the quantizer. The $(2^N \times 2^N)$-matrix of the memory channel is given as

$$\mathbf{P}(j|i) = \begin{bmatrix} P(0|0) & \dots & P(2^N-1|0) \\ \vdots & \ddots & \vdots \\ P(0|2^N-1) & \dots & P(2^N-1|2^N-1) \end{bmatrix} \quad (6)$$

To obtain the transmission matrix P(r|x) of the concatenation of both channels, the index assignment has also to be considered. As it is a mapping of quantizer output to memory channel input, it may be represented by a matrix 5, that permutes the columns of P(r|x) in the required order. The reverse permutation has to be applied to the columns of P(j |i) using the transpose of 5. Then we have the transmission matrix as

$$\mathbf{P}(\bar{r}|x) = \mathbf{P}(r|x)\mathbf{\Pi}\mathbf{P}(j|i)\mathbf{\Pi}^T, \quad (7)$$

Where ∏ is for example given as

$$\mathbf{\Pi} = \begin{bmatrix} & \mathbf{I}_{2^N-1} \\ \mathbf{I}_{2^N-1} & \end{bmatrix} \text{ for Two's complement,} \quad (8)$$

From Eq. (7) it is already apparent that the concatenation of quantized AWGN channel and unreliable buffer memory can be seen as cascade of two DMCs. Figure 2 illustrates this cascade for the case of N = 2 Bit and Two's complement index assignment. It can be noted that the index assignment is just a way of connecting the first DMC to the second one.

To derive the transmission matrix it has intuitively been assumed, as illustrated in Fig. 2, that the output of the memory channel only depends on its input, such that

$$P(\bar{r}|r,x) = P(\bar{r}|r). \quad (9)$$

Now let R, R and X be the random variables representing r, r and x, respectively. Then Eq. (9) is justified by the observation that once R is known, R cannot reveal any additional information about X, because there is no connection between X and R other than the cascade of communication and memory channel. This means that the MI of X and R conditioned on R vanishes,

$$I(X;\bar{R}|R) = 0, \quad (10)$$

Thus in order to optimize the MI I (X;R) and with it the MI loss due to the memory channel, all system parameters have to be jointly taken into account. Therefore, the optimization should be carried out subject to the quantizer (represented by the scaler γ) and the index assignment 5. This approach is investigated in the following section for a Turbo decoding scenario.

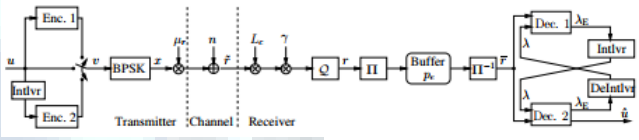

Fig. 3. System model for Turbo coded transmission with unreliable received and LLR buffer

2.3 EXIT chart

The influence of optimized index assignment and quantization width N on the decoding behaviour is first studied using EXIT charts. Consider Fig. 4 (right), where the performance of conventional Turbo decoder ("MAP") and FT decoder ("FTMAP") using NBC index assignment (5NBC) are compared for two different quantization widths N = 4 and N = 6 and pe = 0.01. As a reference the chart for a decoder with pe = 0 and identical quantization settings is shown ("Ref.") – given the width of the tunnel, it can be expected that the decoder will converge at this Eb/N0 level. If, however, the received values experience additional distortion due to the memory channel, then the tunnel becomes much smaller and decoding performance will be deteriorated. In Fig. 4 (right), where a quantization width of N = 4 is used, this impact appears like a small SNR degradation on the communication channel and manifests as a reduction of the EXIT tunnel. It can also be observed, that in this case, there is only very little difference between the conventional decoder and the fault tolerant decoder, and only very close observation reveals the slight improvement due to latter. Convergence to BERs smaller than about 0.08 cannot be expected for both decoders. However, increasing the quantization width to N = 6 Bit, as shown Fig. 5, leads to a significant difference between both decoders: The

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conventional decoder exhibits a substantial performance degradation, which is indicated by a very early crossing of the EXIT curves. In fact even for very good a priori information (I (X;3) → 1), the decoder is not capable of producing improved extrinsic information, such that decoding performance is expected to be strongly degraded. The FT decoder on the other hand shows an improved EXIT chart compared to the N = 4 case: While the tunnel is still considerably smaller than for the reference, the curves do not intersect and given a sufficient number of iterations the decoder may be able to achieve reference BER performance. Thus it can be concluded that while an increased quantization width amplifies the impact of the memory channel and degrades performance of a conventional decoder, it also enables improved error-resilience due to increased redundancy in quantizer output. Exploitation of this redundancy requires the FT decoder though. As suggested by Fig. 4 (left) a higher quantization width and an optimized index assignment w.r.t. Eq. (18) can yield further improvement. Figures 6 and 7 therefore compare EXIT charts of the FT decoder for NBC (5NBC) and optimized index assignments (5∗). In Fig. 6 a quantization width of N = 4 is employed. The limited redundancy in R and smaller degrees of freedom during the optimization do not allow for any gain of the optimized index assignment over NBC in this case. Both charts are identical. But with N increased by two Bit, the optimization becomes more effective as shown in Fig. 7. The tunnel nearly approaches the reference, indicating that the decoder will converge with less iterations than in the NBC case. A general observation from the presented EXIT charts is that an unreliable receive buffer leads to degradation in the lower to medium part of the chart. This is due to the fact that during the ongoing decoding process the extrinsic LLRs become more important than the received values. Regarding the BER performance, we thus expect a degradation of decoding threshold but only marginal impact on the error floor, because low BERs are represented by the very upper part of the chart, where the received values only have small impact.

IV. SIMULATION RESULTS

In this section simulation results for EXIT charts and BER are shown. The BER simulation follows the system as shown in Fig. 1. All results are based on a binary rate R = 1/3 Turbo code using parallel concatenation of two UMTS/LTE compatible [1] recursive systematic encoders G(D) = h 1, 1+D+D3 1+D2+D3 i . BPSK mapped symbols with gain factor μ = 1 are then transmitted over an AWGN channel. The scaling factor γ ∗ is selected depending on the current Eb/N0 using (14), with parameters (m, c) as (−0.09, 0.77), (−0.09, 1.16) and (−0.08, 1.56) for pe = 0, pe = 0.01 and pe = 0.05, respectively. In all cases quantization of the received values is done using Nr = 4 bit with two's complement representation. Two's complement is equivalent to NBC IA, which according to the results from Sec. III-B is only slightly worse than optimized IA in terms of the resulting MI I(X; R). For the LLRs λ a Nλ = 7 bit quantizer is used, where dλ = 5 and fλ = 2. The Turbo decoder uses the FT MAP as described in Sec. III-A based on the

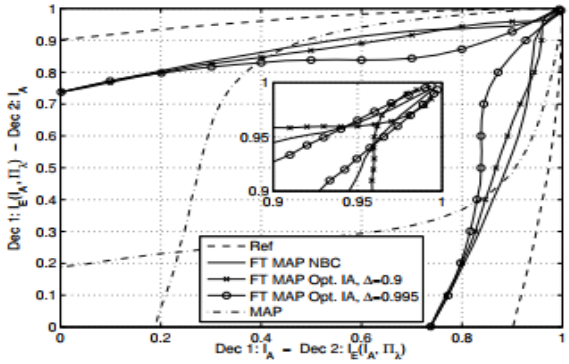

Fig. 4. EXIT chart for conventional MAP and FT MAP with different IA (Eb/N0 = 4dB, pe = 0.05)

LogMAP algorithm with 8 iterations. The required LUTs are precomputed assuming perfect knowledge of the parameters pe, σ 2 and σ 2 λ . Figs. 7 and 8 compare the EXIT charts and BER of a decoder based on the FT MAP to a conventional MAP. For the FT MAP, three cases are considered: NBC IA, and optimized IA with Δ = 0.9 and Δ = 0.995. Additionally, results for a decoder with error-free buffer memory are shown as a reference ("Ref"). Looking at Fig. 4 it is obvious that the EXIT chart of the conventional MAP decoder in case of erroneous buffer memory (pe = 0.05) is strongly degraded: The early crossing point of both curves indicates that the decoding process will not converge at the given SNR. A significantly higher SNR would be required for convergence. On the other hand, the curves of the FT MAP based decoder using NBC IA do not intersect at all, such that an improved BER can be expected. The effect of using an IA based on optimizing (15) can also be observed clearly: For Δ = 0.9, the region IA > 0.9 is disregarded during optimization, which leads to an intersection at about 0.96, but also to a wider "bottleneck", which is supposed to increase robustness of the decoder. On the other hand, for Δ = 0.995 the "bottleneck" is smaller in the region IA < 0.94, but improved in the very upper part. This leads to better performance for higher SNR and possibly an improved error floor. The BER curves in Fig. 8 confirm these conclusions. Considering for example a BER working point of 10−4 and pe = 0.05 (blue curves), the Turbo decoder based on the conventional MAP algorithm shows a performance loss of about 7dB compared to the reference. The FT MAP based decoder significantly improves the BER performance: A performance gain of 3dB is reached by using NBC IA. The optimized IA with Δ = 0.995 is improved by another 0.4dB, while the optimized IA

with Δ = 0.9 is degraded by about 1dB. However, if the latter IA is used, a BER of 10−2 is already reached at 2.4dB, while NBC IA and the IA optimized for Δ = 0.995 require 2.8dB and 3.6db, respectively. Finally, it can be observed that the FT MAP using NBC IA exhibits an error floor, while there is a significantly lower floor in the considered BER range for the optimized IAs. The same holds for a smaller bit error probability of pe = 0.01 (red curves). It can be concluded that selecting an optimized, fixed IA Πλ with a suitable Δ may outperform NBC IA, depending on the BER requirements, at little implementation cost.

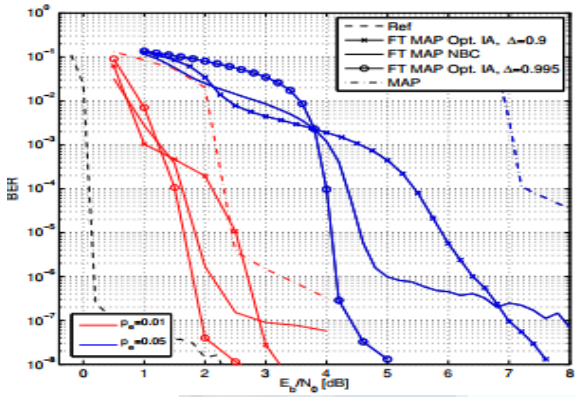

Fig. 8. Comparison of BER performance after 8 iterations for FT MAP and conventional MAP for pe = 0.01 and pe = 0.05, and reference (pe = 0).

V. CONCLUSION

Increasing integration depths of integrated circuits may lead to higher susceptibility against process variations and soft error events. Similarly, aggressive voltage scaling can yield unreliable operation of logic and memory of an integrated circuit. Developing signal processing algorithms that can to some extend deal with unreliable underlying hardware is thus an emerging problem. In this paper a Turbo decoder with an unreliable receive buffer was studied. This buffer is modeled as a binary symmetric channel that acts on the quantized received values. It can thus be seen as an additional discrete memoryless channel that is cascaded to the actual communication channel. The interaction of both channels, represented by quantizer and index assignment, was identified as an important impact factor on the resilience of the Turbo decoder against errors originating from the memory channel. For a decoder with a transition metric adapted to the actual statistical model of the channel cascade, a joint optimization of both components yields improved error-resilience without increasing the computational complexity of the decoder.

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